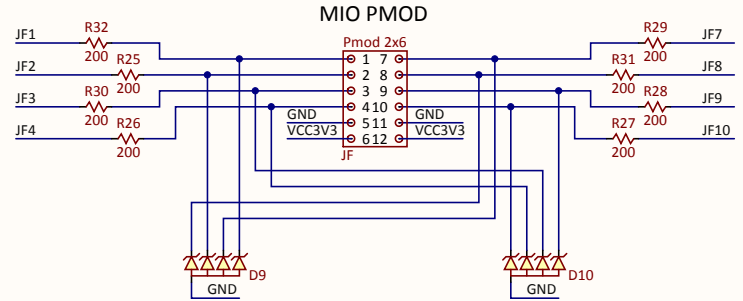
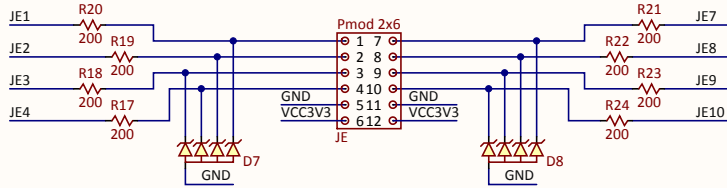
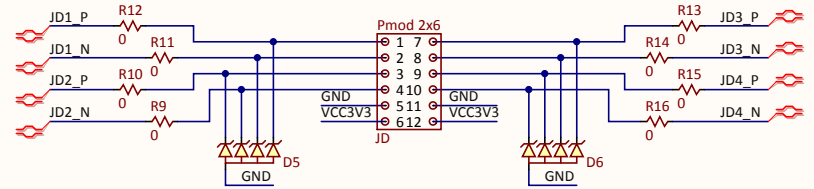
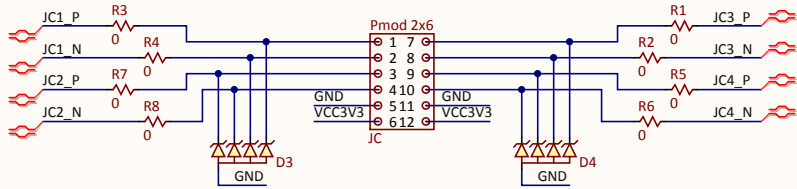
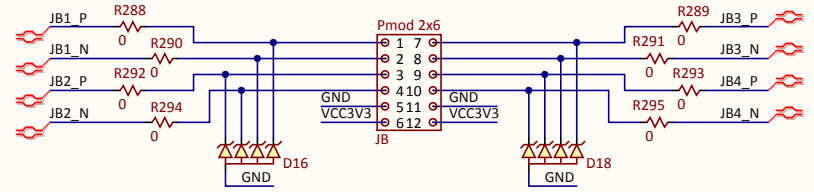
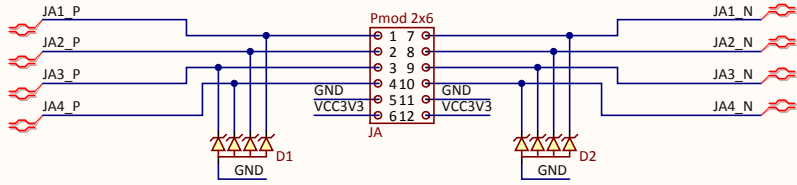
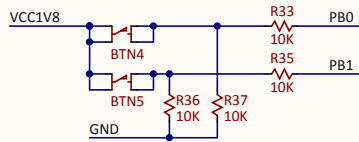


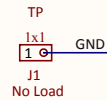
### XADC PMOD



### MIO BUTTON



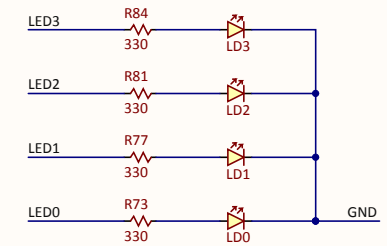
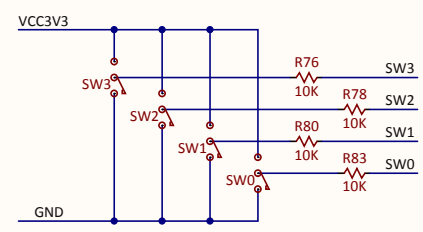
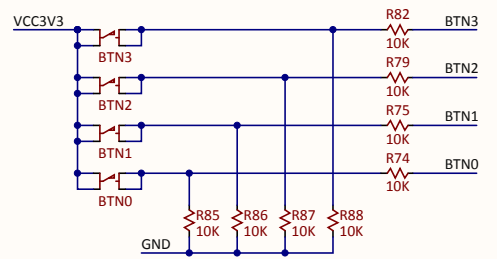
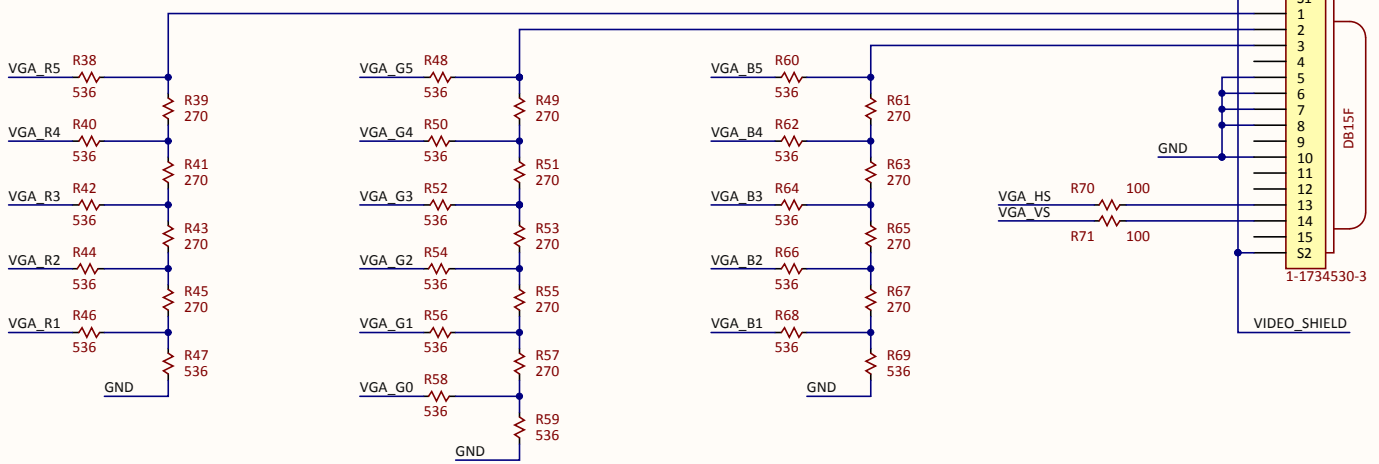
### MIO LED




ZYBO Board | Digilent Inc. | Xilinx | Analog Devices | CE | ROHS | Chinese ROHS

Foot  
F1  
Foot  
F2  
Foot  
F3  
Foot  
F4

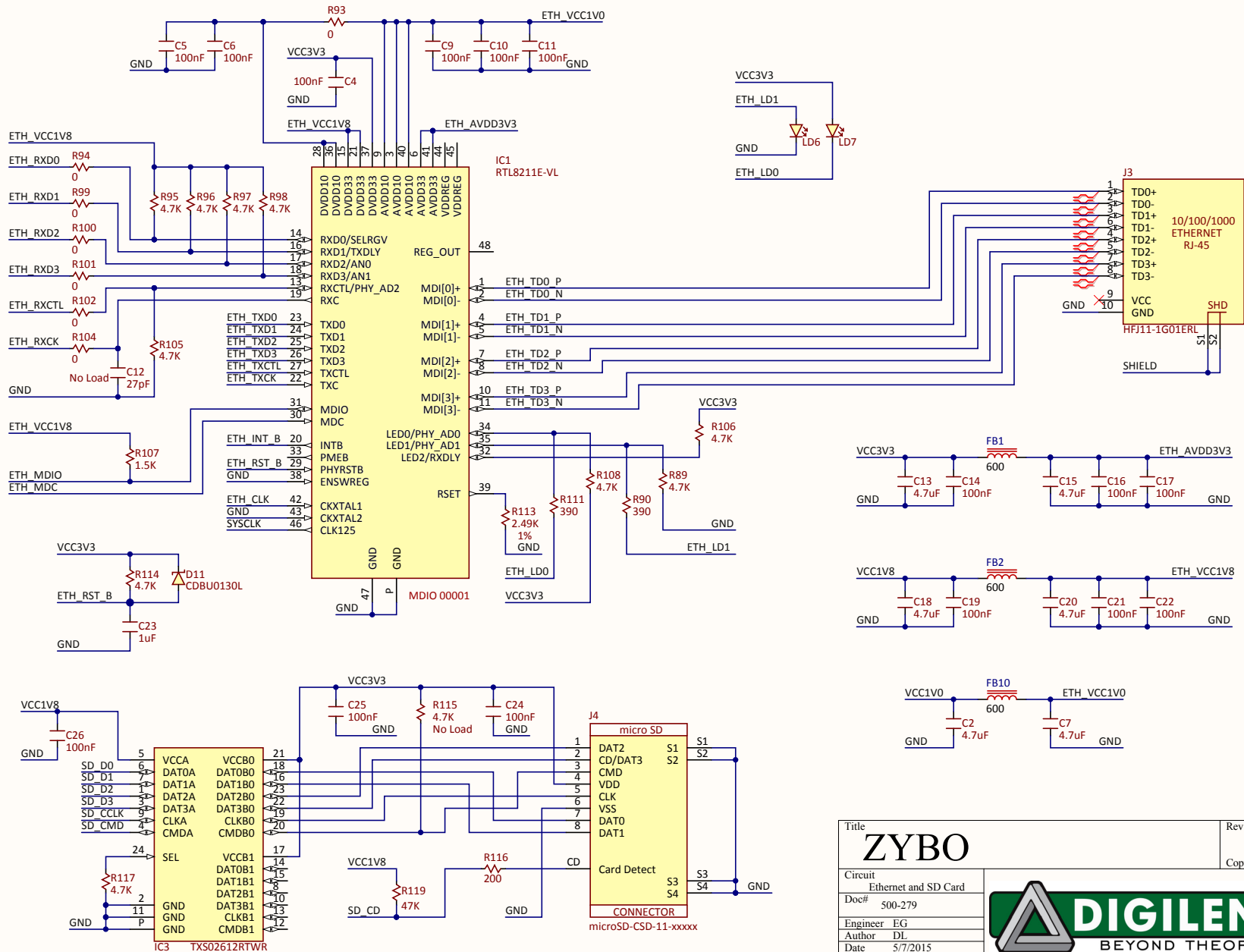
Title <b>ZYBO</b>		Rev <b>B.3</b>
Circuit PMODs, MIO		Copyright 2015
Doc#	500-279	
Engineer	EG	
Author	DL	
Date	5/7/2015	
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<b>ZYBO</b>		<b>B.3</b>	
Circuit		Copyright 2015	
VGA, General I/O			
Doc#	500-279		
Engineer	EG		
Author	DL		
Date	5/7/2015		
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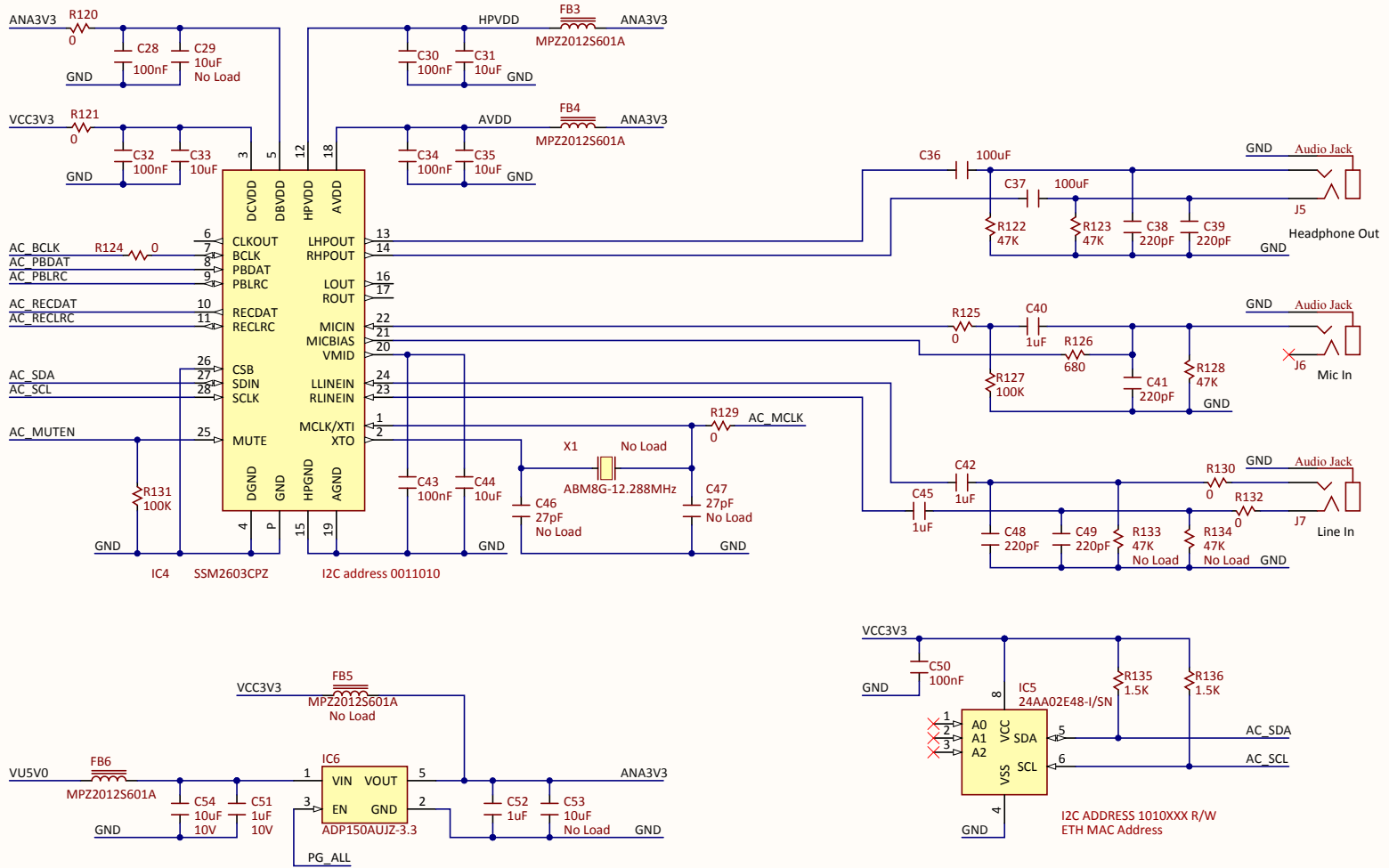
**DIGILENT**  
BEYOND THEORY



Title		<b>ZYBO</b>	Rev	<b>B.3</b>
Circuit			Ethernet and SD Card	
Doc#		500-279		
Engineer		EG		
Author		DL		
Date		5/7/2015		
Sheet#		3 out of 13		



**DIGILENT**  
BEYOND THEORY



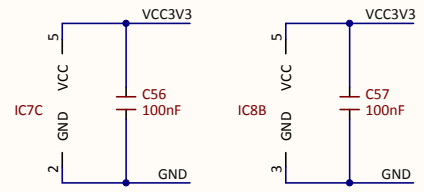
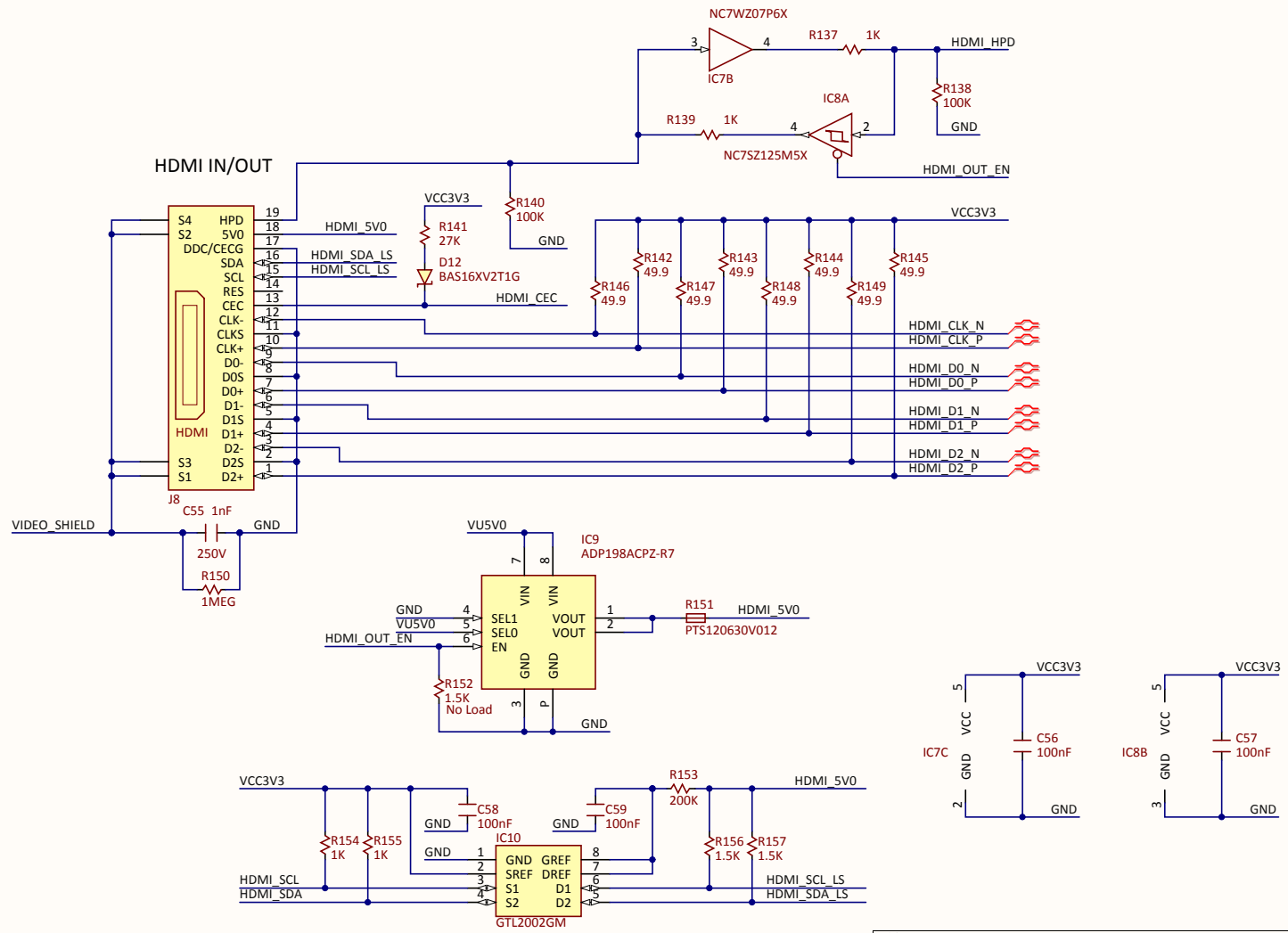
For more information on the parts used in this design, please refer to:

[www.analog.com/ssm2603](http://www.analog.com/ssm2603) (Low Power Audio Codec)

[www.analog.com/adp150](http://www.analog.com/adp150) (Ultra Low Noise, 150 mA CMOS Linear Regulator)

Title		Rev	
ZYBO		B.3	
Circuit		Copyright 2015	
Audio Codec, EUI EEPROM			
Doc# 500-279			
Engineer EG			
Author DL			
Date 5/7/2015			
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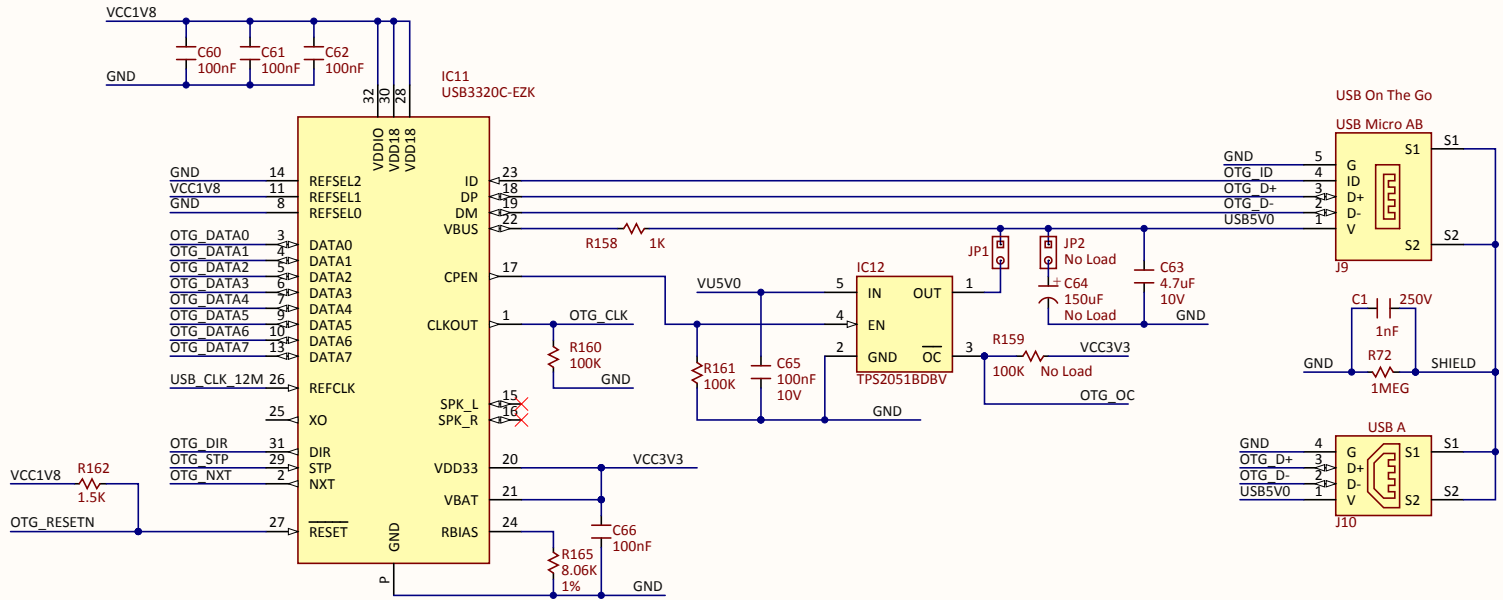






Title		<b>ZYBO</b>		Rev	<b>B.3</b>
Circuit		HDMI		Copyright	2015
Doc#	500-279				
Engineer	EG				
Author	DL				
Date	5/7/2015				
Sheet#	5	out of	13		

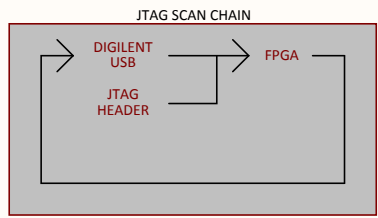
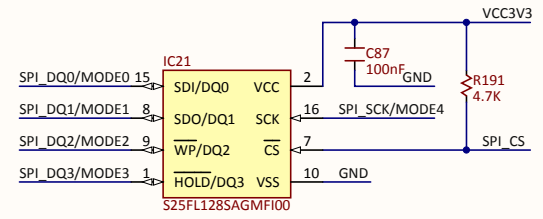
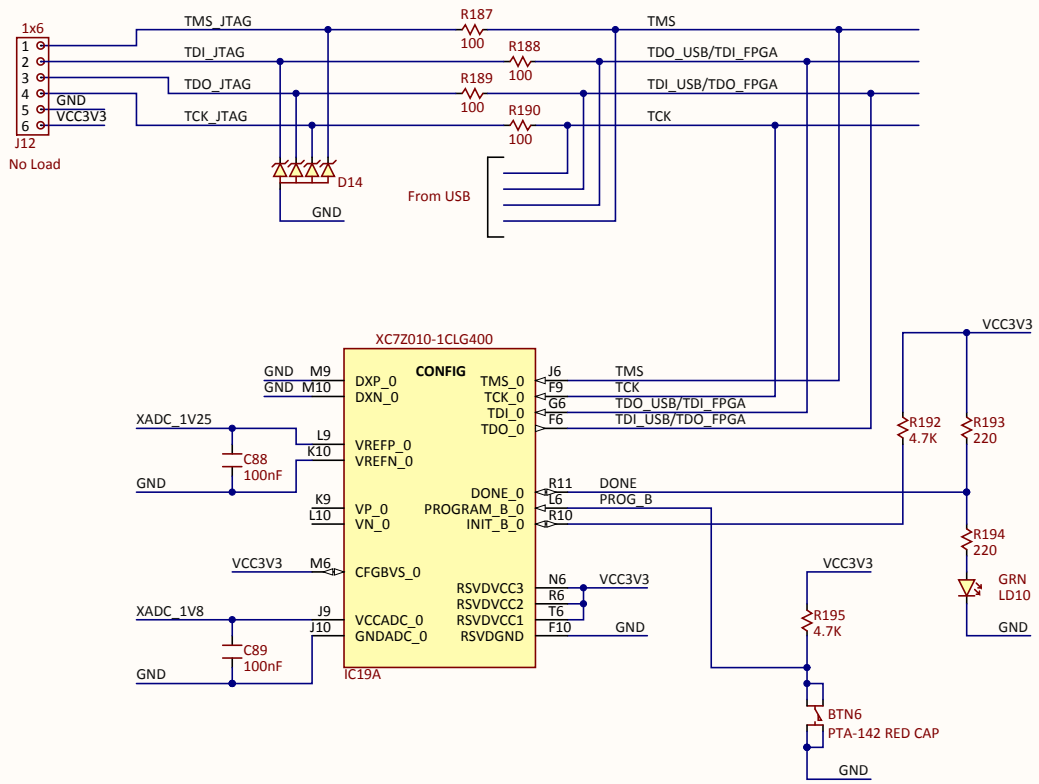


For more information on the parts used in this design, please refer to:  
[www.analog.com/adp198](http://www.analog.com/adp198) (Logic Controlled, 1 A, High-Side Load Switch with Reverse Current Blocking)



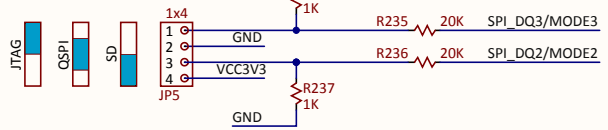
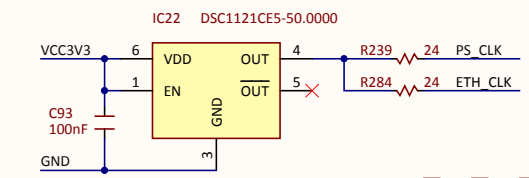
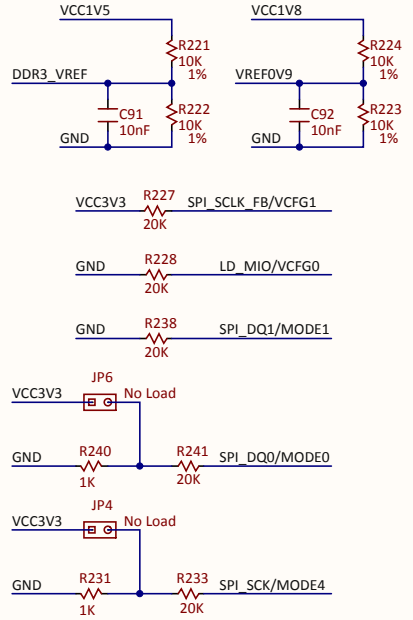
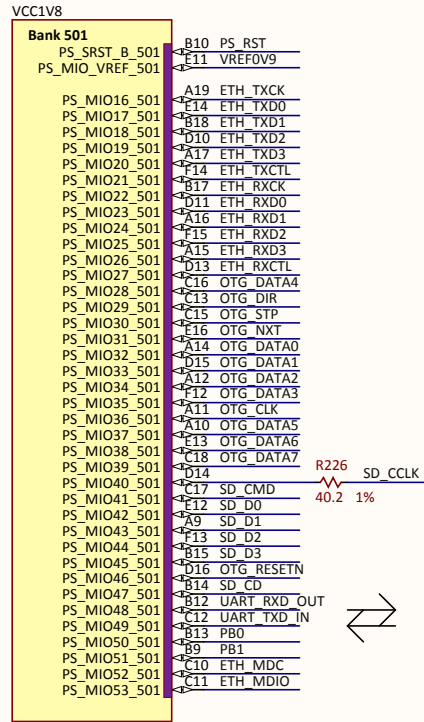
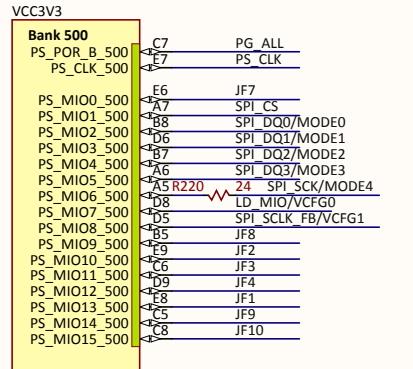
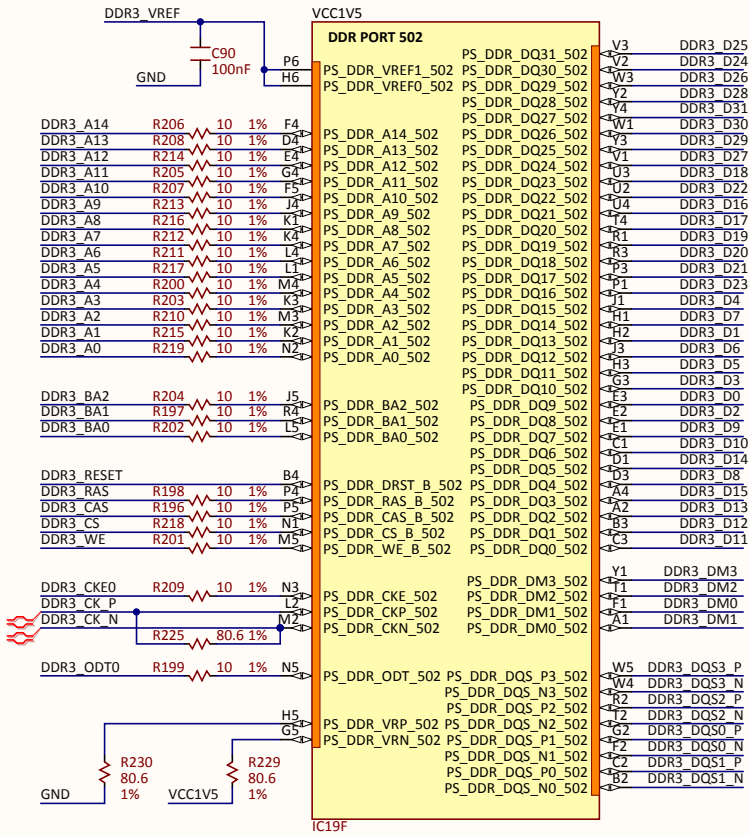
Title			Rev
ZYBO			B.3
Circuit	USB OTG	Copyright 2015	
Doc#	500-279		
Engineer	EG		
Author	DL		
Date	5/7/2015		
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Title		Rev
<b>ZYBO</b>		<b>B.3</b>
Circuit		Copyright 2015
FPGA Configuration, Flash		
Doc#	500-279	
Engineer	EG	
Author	DL	
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Title		<b>ZYBO</b>	Rev
Circuit			
Doc#		500-279	Copyright 2015
Engineer		EG	
Author		DL	
Date		5/7/2015	
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VCC3V3

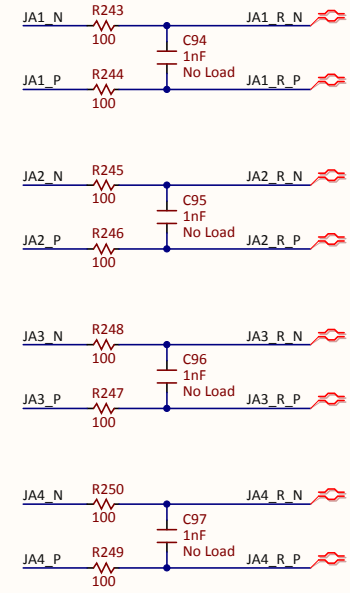
BANK 34	
IO_0_34	R19 VGA_VS
IO_L1P_T0_34	T11 JC2_P
IO_L1N_T0_34	T10 JC2_N
IO_L2P_T0_34	T12 JC4_P
IO_L2N_T0_34	U12 JC4_N
IO_L3P_T0_DQS_PUDC_B_34	U13 OTG_OC
IO_L3N_T0_DQS_34	V13 JE7
IO_L4P_T0_34	V12 JE1
IO_L4N_T0_34	W13 SW2
IO_L5P_T0_34	T14 JD1_P
IO_L5N_T0_34	T15 JD1_N
IO_L6P_T0_34	P14 JD2_P
IO_L6N_T0_VREF_34	R14 JD2_N
IO_L7P_T1_34	V16 BTN3
IO_L7N_T1_34	V17 JE10
IO_L8P_T1_34	W14 JC3_P
IO_L8N_T1_34	V14 JC3_N
IO_L9P_T1_DQS_34	T16 SW3
IO_L9N_T1_DQS_34	U17 JE8
IO_L10P_T1_34	V15 JC1_P
IO_L10N_T1_34	W15 JC1_N
IO_L11P_T1_SRCC_34	U14 JD3_P
IO_L11N_T1_SRCC_34	U15 JD3_N
IO_L12P_T1_MRCC_34	U18
IO_L12N_T1_MRCC_34	U19
IO_L13P_T2_MRCC_34	N18 AC_SCL
IO_L13N_T2_MRCC_34	P19 VGA_HS
IO_L14P_T2_SRCC_34	N20 VGA_G1
IO_L14N_T2_SRCC_34	P20 VGA_B1
IO_L15P_T2_DQS_34	T20 JB1_P
IO_L15N_T2_DQS_34	U20 JB1_N
IO_L16P_T2_34	V20 JB2_P
IO_L16N_T2_34	W20 JB2_N
IO_L17P_T2_34	V18 JB3_P
IO_L17N_T2_34	V19 JB3_N
IO_L18P_T2_34	V16 BTN2
IO_L18N_T2_34	W16 JE2
IO_L19P_T3_34	R16
IO_L19N_T3_VREF_34	R17
IO_L20P_T3_34	T17 JE9
IO_L20N_T3_34	R18 BTNO
IO_L21P_T3_DQS_34	V17 JD4_P
IO_L21N_T3_DQS_34	V18 JD4_N
IO_L22P_T3_34	W18 JB4_P
IO_L22N_T3_34	W19 JB4_N
IO_L23P_T3_34	N17 AC_SDA
IO_L23N_T3_34	P18 AC_MUTEN
IO_L24P_T3_34	P15 SW1
IO_L24N_T3_34	P16 BTN1
IO_25_34	T19 AC_MCLK


IC19B

VCC3V3

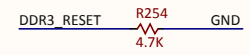
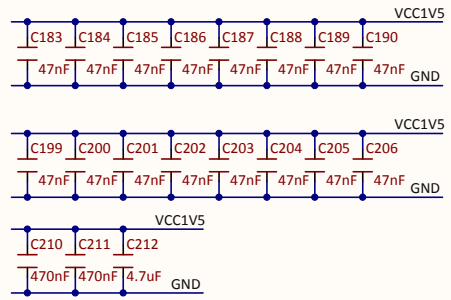
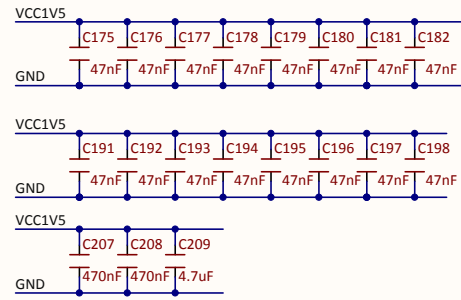
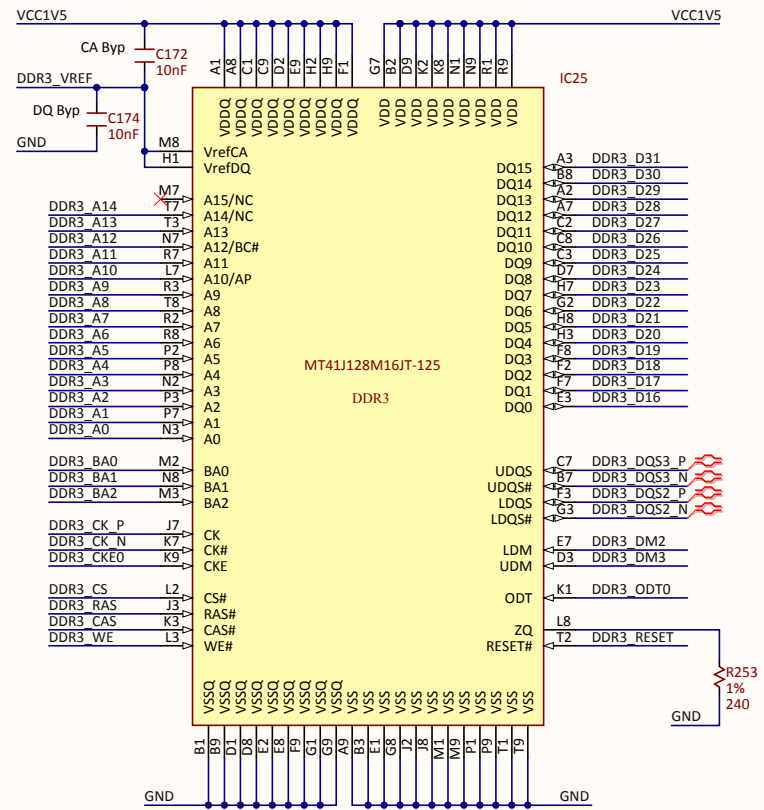
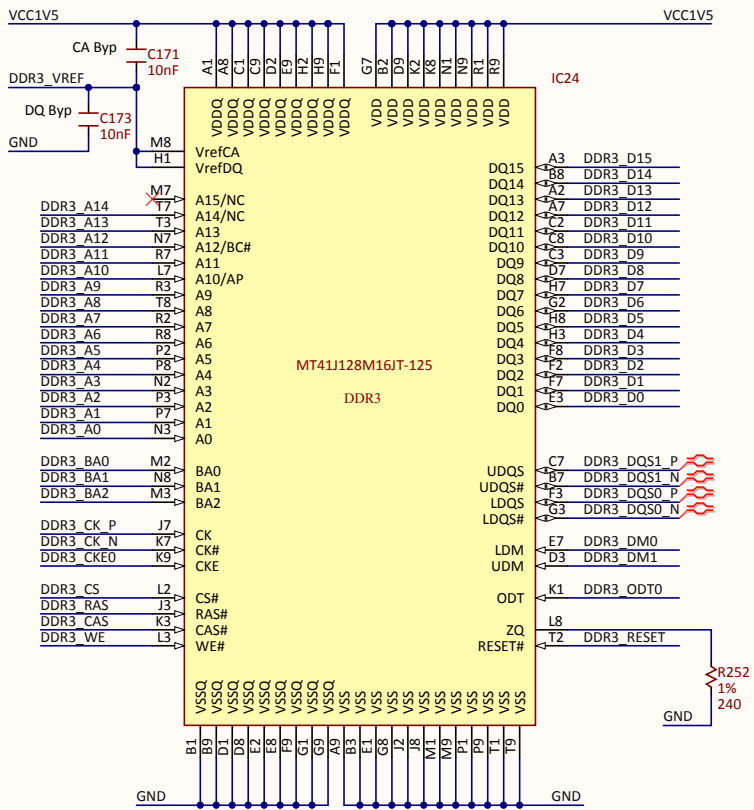
BANK 35	
IO_0_35	G14 LED2
IO_L1P_T0_AD0P_35	C20 HDMI_D1_P
IO_L1N_T0_AD0N_35	B20 HDMI_D1_N
IO_L2P_T0_AD8P_35	B19 HDMI_D2_P
IO_L2N_T0_AD8N_35	A20 HDMI_D2_N
IO_L3P_T0_DQS_AD1P_35	E17 ETH_RST_B
IO_L3N_T0_DQS_AD1N_35	D18 LED3
IO_L4P_T0_35	D19 HDMI_D0_P
IO_L4N_T0_35	D20 HDMI_D0_N
IO_L5P_T0_AD9P_35	E18 HDMI_HPD
IO_L5N_T0_AD9N_35	E19 HDMI_CEC
IO_L6P_T0_35	F16 ETH_INT_B
IO_L6N_T0_VREF_35	F17 HDMI_OUT_EN
IO_L7P_T1_AD2P_35	M19 VGA_R1
IO_L7N_T1_AD2N_35	M20 VGA_B2
IO_L8P_T1_AD10P_35	M17 AC_PBDAT
IO_L8N_T1_AD10N_35	M18 AC_RECLRC
IO_L9P_T1_DQS_AD3P_35	L19 VGA_G2
IO_L9N_T1_DQS_AD3N_35	L20 VGA_R2
IO_L10P_T1_AD11P_35	K19 VGA_B3
IO_L10N_T1_AD11N_35	L19 VGA_G3
IO_L11P_T1_SRCC_35	L16 SYSCLK
IO_L11N_T1_SRCC_35	L17 AC_PBLRC
IO_L12P_T1_MRCC_35	K17 AC_RECCLK
IO_L12N_T1_MRCC_35	K18 AC_BCLK
IO_L13P_T2_MRCC_35	H16 HDMI_CLK_P
IO_L13N_T2_MRCC_35	H17 HDMI_CLK_N
IO_L14P_T2_AD4P_SRCC_35	I18 VGA_B4
IO_L14N_T2_AD4N_SRCC_35	H18 VGA_G0
IO_L15P_T2_DQS_AD12P_35	F19 VGA_R5
IO_L15N_T2_DQS_AD12N_35	F20 VGA_G5
IO_L16P_T2_35	G17 HDMI_SCL
IO_L16N_T2_35	G18 HDMI_SDA
IO_L17P_T2_AD5P_35	J20 VGA_R3
IO_L17N_T2_AD5N_35	H20 VGA_G4
IO_L18P_T2_AD13P_35	G19 VGA_B5
IO_L18N_T2_AD13N_35	G20 VGA_R4
IO_L19P_T3_35	H15 JE4
IO_L19N_T3_VREF_35	G15 SW0
IO_L20P_T3_AD6P_35	K14 JA4_R_P
IO_L20N_T3_AD6N_35	J14 JA4_R_N
IO_L21P_T3_DQS_AD14P_35	N15 JA1_R_P
IO_L21N_T3_DQS_AD14N_35	N16 JA1_R_N
IO_L22P_T3_AD7P_35	L14 JA2_R_P
IO_L22N_T3_AD7N_35	L15 JA2_R_N
IO_L23P_T3_35	M14 LED0
IO_L23N_T3_35	M15 LED1
IO_L24P_T3_AD15P_35	K16 JA3_R_P
IO_L24N_T3_AD15N_35	L16 JA3_R_N
IO_25_35	L15 JE3

IC19C

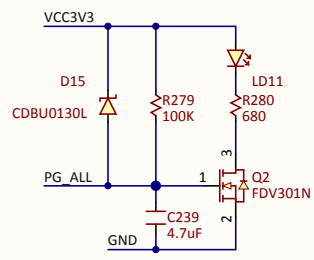
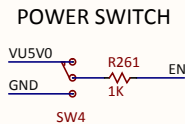
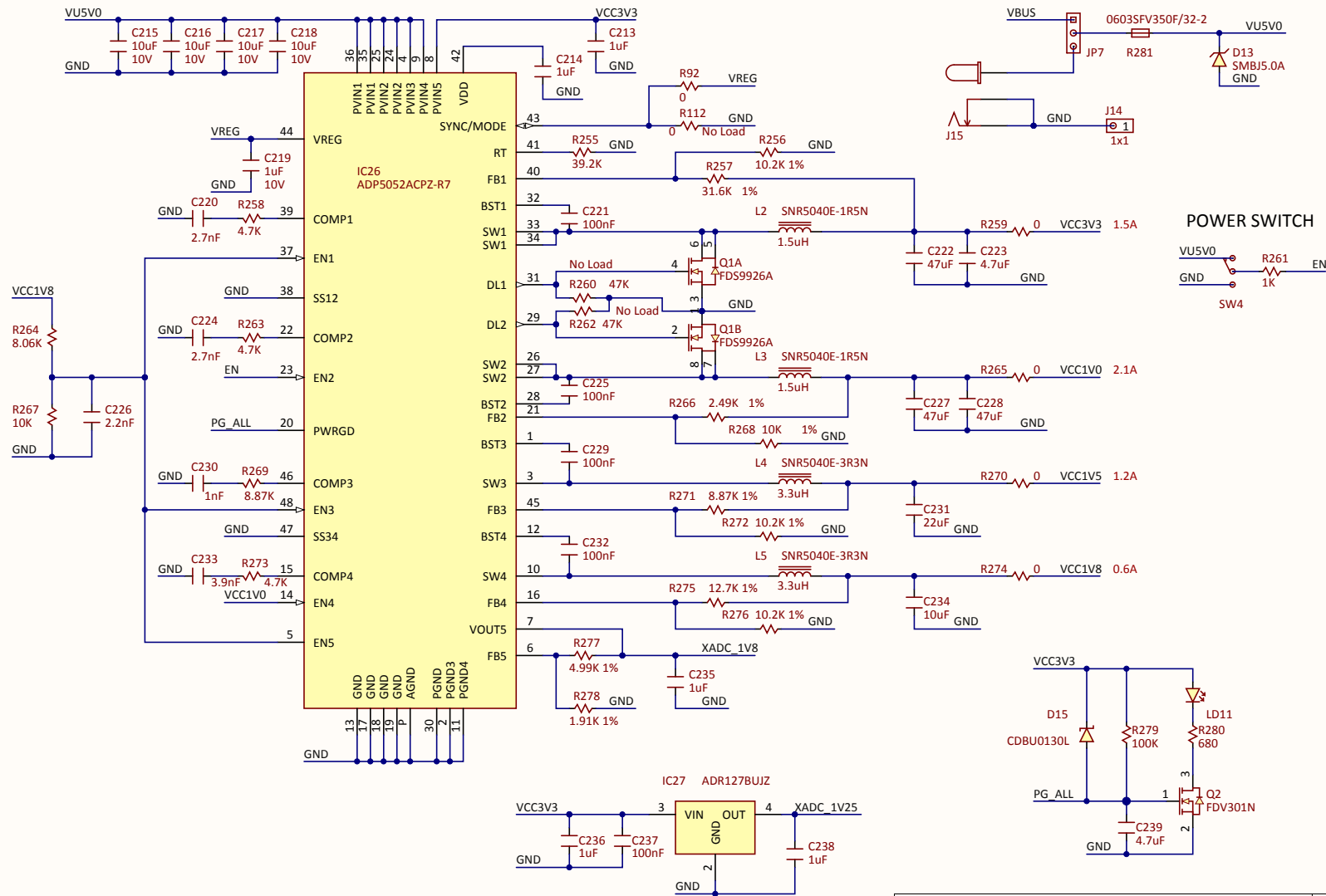


Title		Rev	
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Circuit		Copyright 2015	
FPGA Banks, Anti Alias Filters			
Doc#	500-279		
Engineer	EG		
Author	DL		
Date	5/7/2015		
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Title <b>ZYBO</b>		Rev <b>B.3</b>
Circuit DDR3 Memory		Copyright 2015
Doc# 500-279		
Engineer EG		
Author DL		
Date 5/7/2015		
Sheet# 12 out of 13		



For more information on the parts used in this design, please refer to:

[www.analog.com/adp5052](http://www.analog.com/adp5052) (5 - Channel Integrated Power Solution with Quad Buck Regulators and 200 mA LDO Regulator )

[www.analog.com/adr127](http://www.analog.com/adr127) (Precision, Micropower LDO 1.25 VOUT Voltage Reference )

Title			Rev
Circuit			B.3
Doc#		Copyright 2015	
Engineer		DL	
Author		EG	
Date		5/7/2015	
Sheet#		13 out of 13	
		BEYOND THEORY	