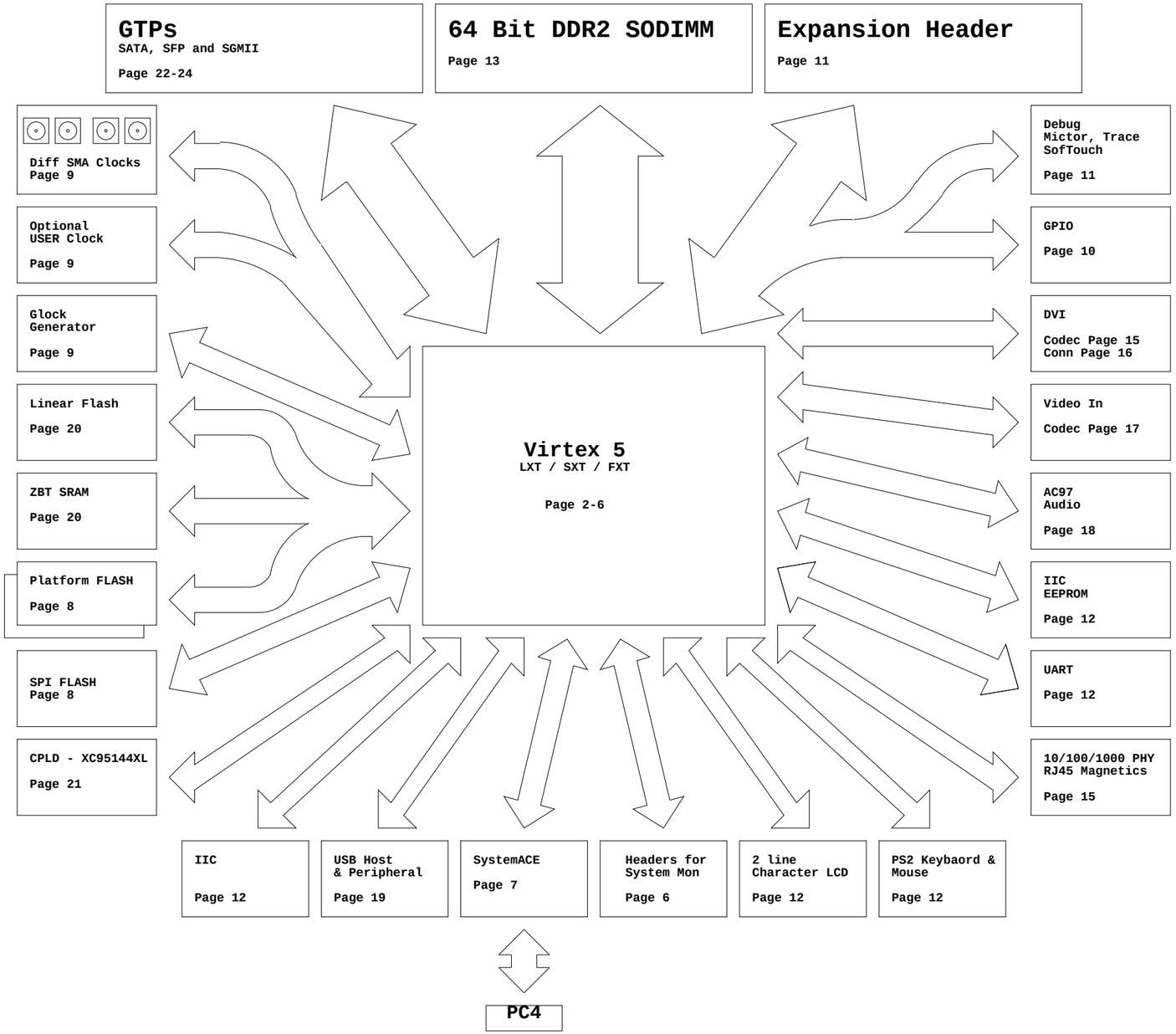
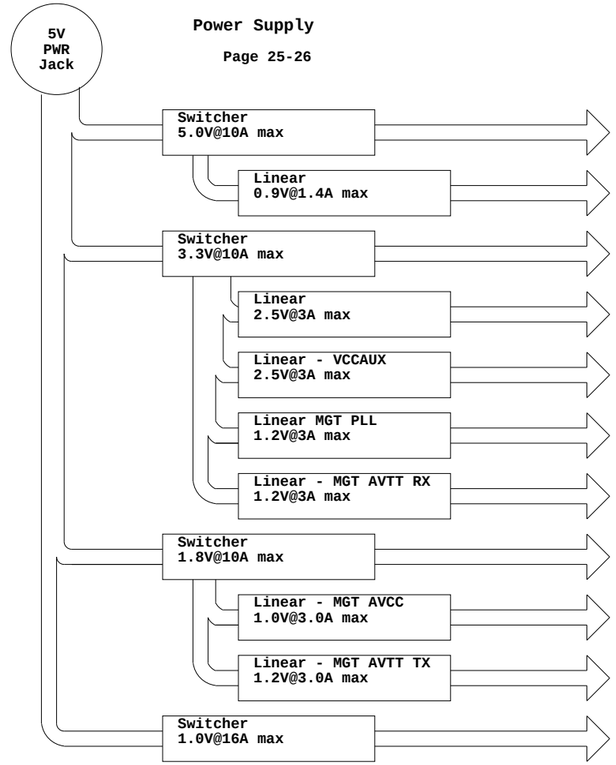
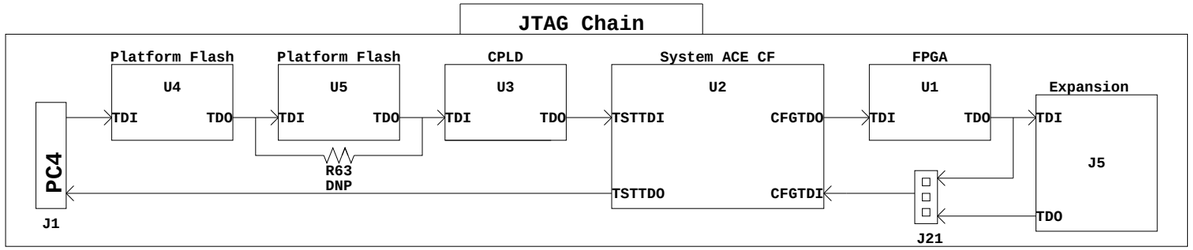
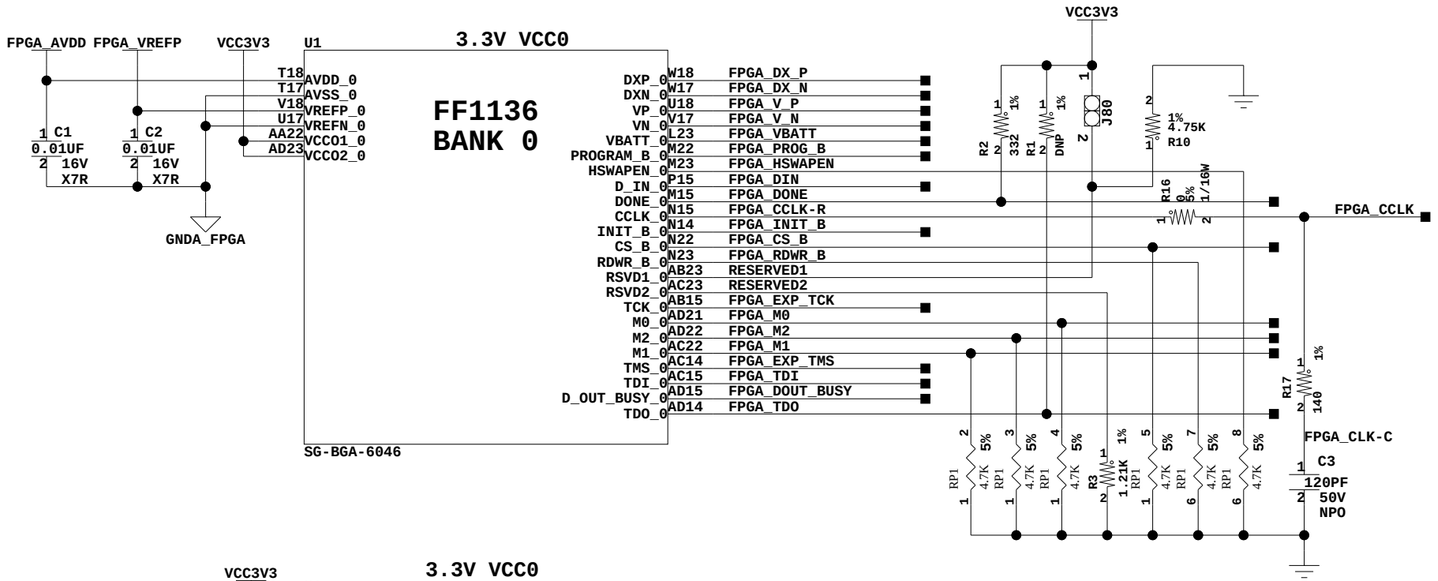


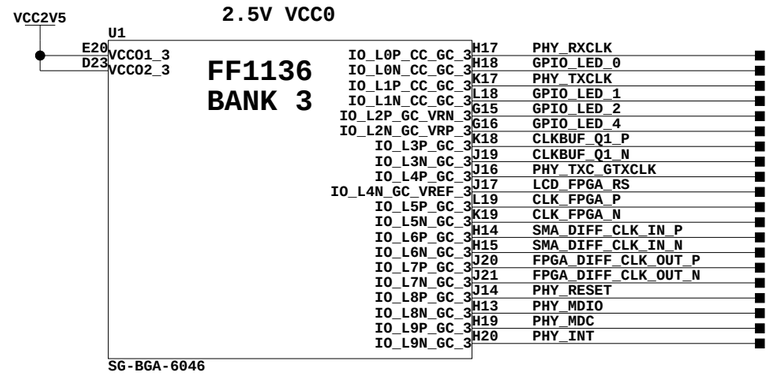


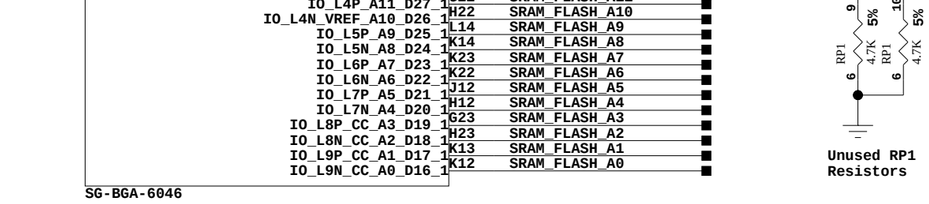


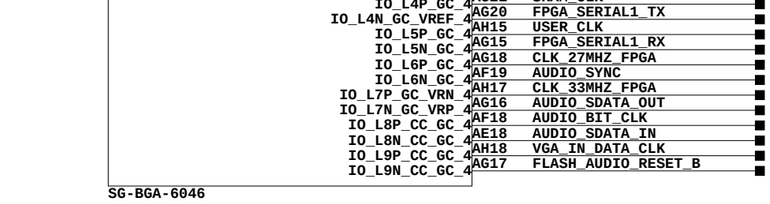
XILINX

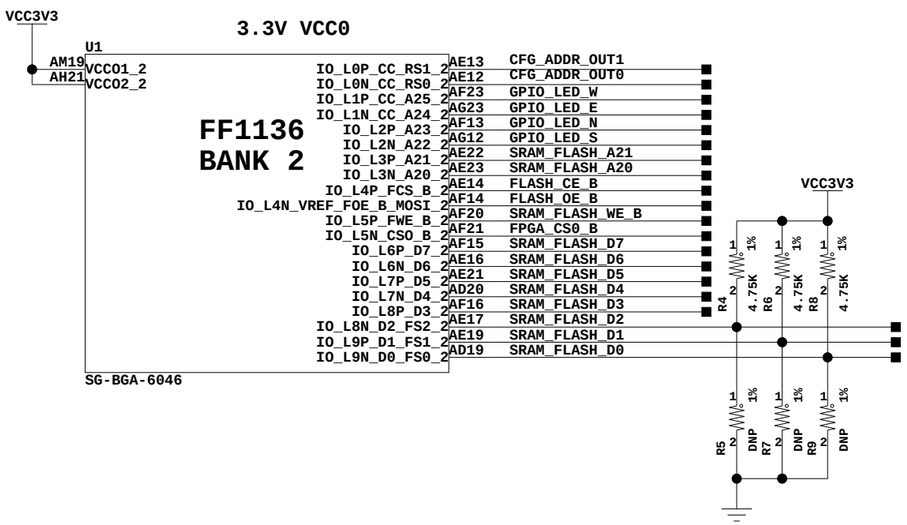
Title:	ML505/6/7 Block Diagram SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	1 of 27	Drawn By	BP







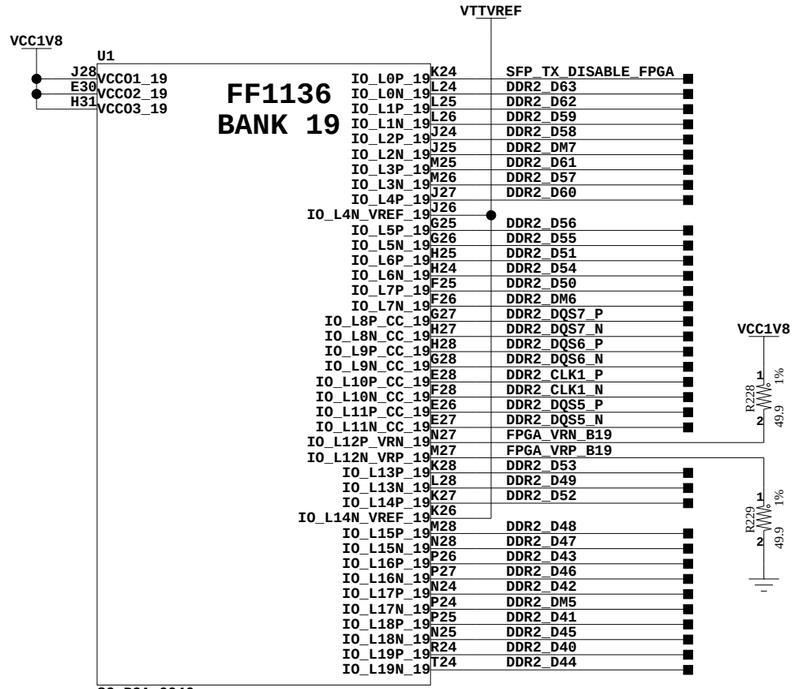


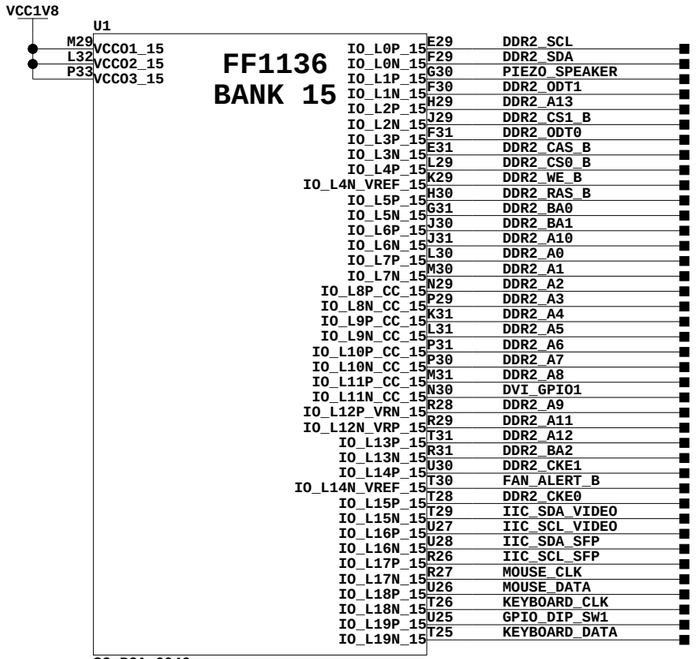


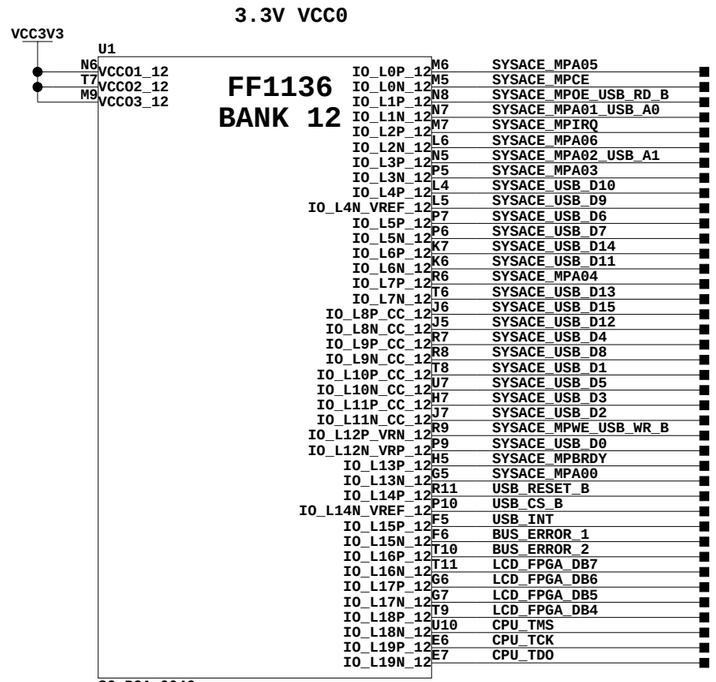
Banks 0,1,2,3,4
Config, FLASH, SRAM, GPIO, CLKs

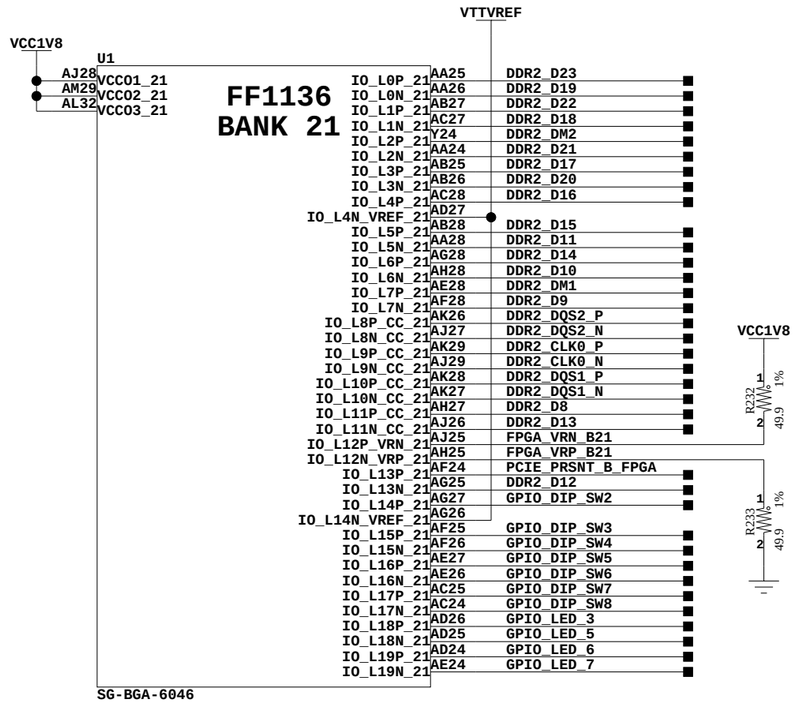
XILINX

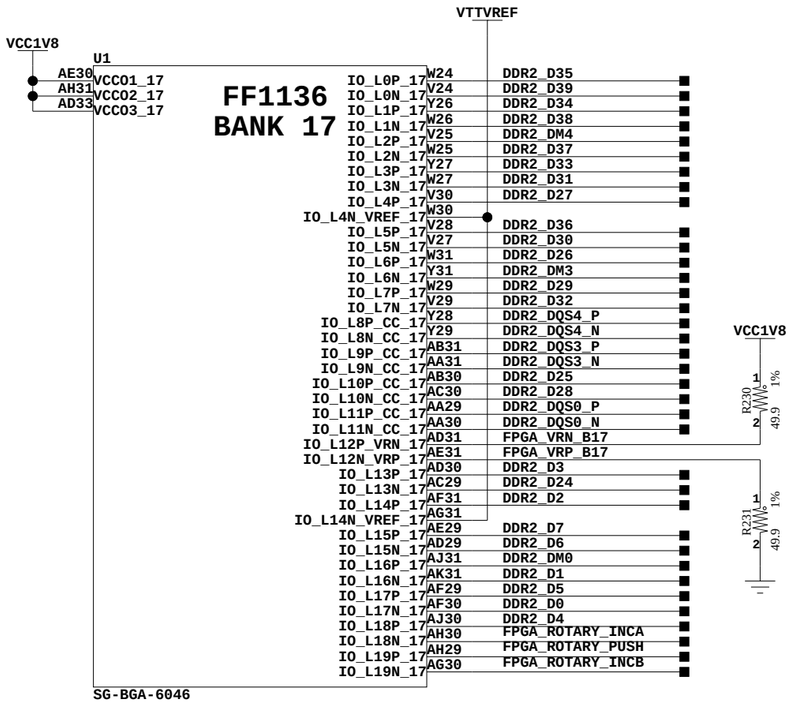
Title:	FPGA Banks 0,1,2,3,4 Config, FLASH, SRAM, GPIO, CLKs SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	2 of 27	Drawn By	BP











Banks 14,16,18,21
DDR2, PS2, GPIO

Title:	FPGA Bank 14, 16, 18, 21DDR2, PS2, GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
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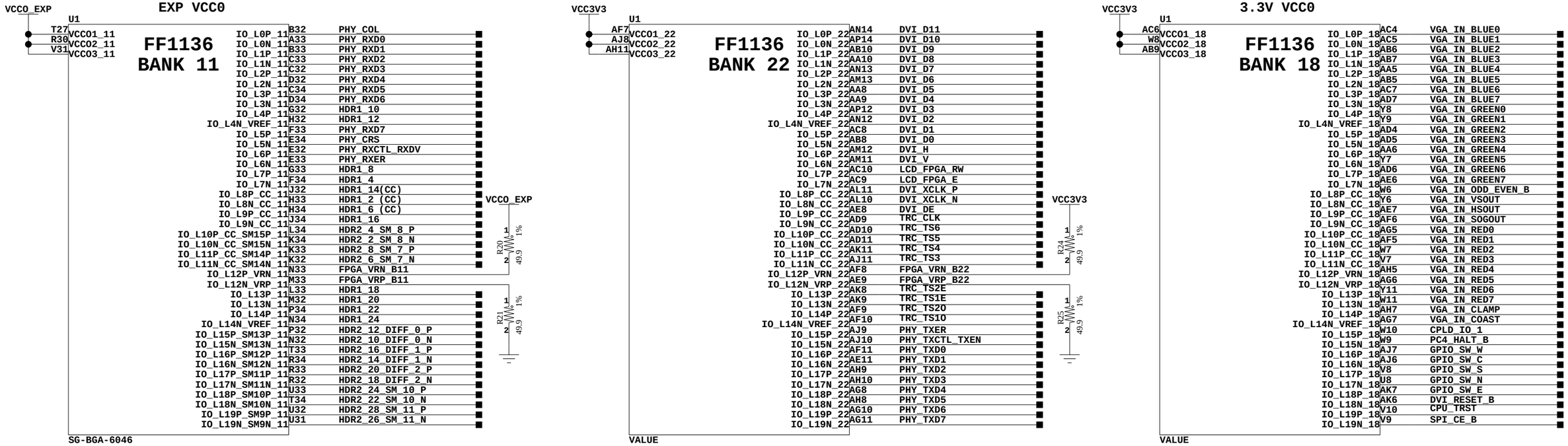
EXP VCC0
VCCO_EXP
U1
FF1136
BANK 11
T27 VCCO1_11
R30 VCCO2_11
V31 VCCO3_11
IO_L0P_11 B32 PHY_COL
IO_L0N_11 A33 PHY_RXD0
IO_L1P_11 B33 PHY_RXD1
IO_L1N_11 C33 PHY_RXD2
IO_L2P_11 C32 PHY_RXD3
IO_L2N_11 D32 PHY_RXD4
IO_L3P_11 C34 PHY_RXD5
IO_L3N_11 D34 PHY_RXD6
IO_L4P_11 G32 HDR1_10
IO_L4N_VREF_11 H32 HDR1_12
IO_L5P_11 F33 PHY_RXD7
IO_L5N_11 E34 PHY_CRS
IO_L6P_11 E32 PHY_RXCTL_RXDV
IO_L6N_11 E33 PHY_RXER
IO_L7P_11 G33 HDR1_8
IO_L7N_11 F34 HDR1_4
IO_L8P_CC_11 J32 HDR1_14(CC)
IO_L8N_CC_11 H33 HDR1_2 (CC)
IO_L9P_CC_11 H34 HDR1_6 (CC)
IO_L9N_CC_11 J34 HDR1_16
IO_L10P_CC_SM15P_11 L34 HDR2_4_SM_8_P
IO_L10N_CC_SM15N_11 K34 HDR2_2_SM_8_N
IO_L11P_CC_SM14P_11 K33 HDR2_8_SM_7_P
IO_L11N_CC_SM14N_11 K32 HDR2_6_SM_7_N
IO_L12P_VRN_11 N33 FPGA_VRN_B11
IO_L12N_VRP_11 M33 FPGA_VRP_B11
IO_L13P_11 L33 HDR1_18
IO_L13N_11 M32 HDR1_20
IO_L14P_11 P34 HDR1_22
IO_L14N_VREF_11 N34 HDR1_24
IO_L15P_SM13P_11 P32 HDR2_12_DIFF_0_P
IO_L15N_SM13N_11 N32 HDR2_10_DIFF_0_N
IO_L16P_SM12P_11 T33 HDR2_16_DIFF_1_P
IO_L16N_SM12N_11 R34 HDR2_14_DIFF_1_N
IO_L17P_SM11P_11 R33 HDR2_20_DIFF_2_P
IO_L17N_SM11N_11 R32 HDR2_18_DIFF_2_N
IO_L18P_SM10P_11 U33 HDR2_24_SM_10_P
IO_L18N_SM10N_11 T34 HDR2_22_SM_10_N
IO_L19P_SM9P_11 U32 HDR2_28_SM_11_P
IO_L19N_SM9N_11 U31 HDR2_26_SM_11_N
VCCO_EXP
R20 49.9 1%
R21 49.9 1%
SG-BGA-6046
VCC3V3
3.3V VCC0
U1
FF1136
BANK 22
AF7 VCCO1_22
AJ8 VCCO2_22
AH11 VCCO3_22
IO_L0P_22 AN14 DVI_D11
IO_L0N_22 AP14 DVI_D10
IO_L1P_22 AB10 DVI_D9
IO_L1N_22 AA10 DVI_D8
IO_L2P_22 AN13 DVI_D7
IO_L2N_22 AM13 DVI_D6
IO_L3P_22 AA8 DVI_D5
IO_L3N_22 AA9 DVI_D4
IO_L4P_22 AP12 DVI_D3
IO_L4N_VREF_22 AN12 DVI_D2
IO_L5P_22 AC8 DVI_D1
IO_L5N_22 AB8 DVI_D0
IO_L6P_22 AM12 DVI_H
IO_L6N_22 AM11 DVI_V
IO_L7P_22 AC10 LCD_FPGA_RW
IO_L7N_22 AC9 LCD_FPGA_E
IO_L8P_CC_22 AL11 DVI_XCLK_P
IO_L8N_CC_22 AL10 DVI_XCLK_N
IO_L9P_CC_22 AE8 DVI_DE
IO_L9N_CC_22 AD9 TRC_CLK
IO_L10P_CC_22 AD10 TRC_TS6
IO_L10N_CC_22 AD11 TRC_TS5
IO_L11P_CC_22 AK11 TRC_TS4
IO_L11N_CC_22 AJ11 TRC_TS3
IO_L12P_VRN_22 AF8 FPGA_VRN_B22
IO_L12N_VRP_22 AE9 FPGA_VRP_B22
IO_L13P_22 AK8 TRC_TS2E
IO_L13N_22 AK9 TRC_TS1E
IO_L14P_22 AF9 TRC_TS2O
IO_L14N_VREF_22 AF10 TRC_TS1O
IO_L15P_22 AJ9 PHY_TXER
IO_L15N_22 AJ10 PHY_TXCTL_TXEN
IO_L16P_22 AF11 PHY_TXD0
IO_L16N_22 AE11 PHY_TXD1
IO_L17P_22 AH9 PHY_TXD2
IO_L17N_22 AH10 PHY_TXD3
IO_L18P_22 AG8 PHY_TXD4
IO_L18N_22 AH8 PHY_TXD5
IO_L19P_22 AG10 PHY_TXD6
IO_L19N_22 AG11 PHY_TXD7
VCC3V3
R24 49.9 1%
R25 49.9 1%
VALUE
VCC3V3
3.3V VCC0
U1
FF1136
BANK 18
AC6 VCCO1_18
W8 VCCO2_18
AB9 VCCO3_18
IO_L0P_18 AC4 VGA_IN_BLUE0
IO_L0N_18 AC5 VGA_IN_BLUE1
IO_L1P_18 AB6 VGA_IN_BLUE2
IO_L1N_18 AB7 VGA_IN_BLUE3
IO_L2P_18 AA5 VGA_IN_BLUE4
IO_L2N_18 AB5 VGA_IN_BLUE5
IO_L3P_18 AC7 VGA_IN_BLUE6
IO_L3N_18 AD7 VGA_IN_BLUE7
IO_L4P_18 Y8 VGA_IN_GREEN0
IO_L4N_VREF_18 Y9 VGA_IN_GREEN1
IO_L5P_18 AD4 VGA_IN_GREEN2
IO_L5N_18 AD5 VGA_IN_GREEN3
IO_L6P_18 AA6 VGA_IN_GREEN4
IO_L6N_18 Y7 VGA_IN_GREEN5
IO_L7P_18 AD6 VGA_IN_GREEN6
IO_L7N_18 AE6 VGA_IN_GREEN7
IO_L8P_CC_18 W6 VGA_IN_ODD_EVEN_B
IO_L8N_CC_18 V6 VGA_IN_VSOUT
IO_L9P_CC_18 AE7 VGA_IN_HSOUT
IO_L9N_CC_18 AF6 VGA_IN_SOGOUT
IO_L10P_CC_18 AG5 VGA_IN_RED0
IO_L10N_CC_18 AF5 VGA_IN_RED1
IO_L11P_CC_18 W7 VGA_IN_RED2
IO_L11N_CC_18 V7 VGA_IN_RED3
IO_L12P_VRN_18 AH5 VGA_IN_RED4
IO_L12N_VRP_18 AG6 VGA_IN_RED5
IO_L13P_18 Y11 VGA_IN_RED6
IO_L13N_18 W11 VGA_IN_RED7
IO_L14P_18 AH7 VGA_IN_CLAMP
IO_L14N_VREF_18 AG7 VGA_IN_COAST
IO_L15P_18 W10 CPLD_IO_1
IO_L15N_18 W9 PC4_HALT_B
IO_L16P_18 AJ7 GPIO_SW_W
IO_L16N_18 AJ6 GPIO_SW_C
IO_L17P_18 V8 GPIO_SW_S
IO_L17N_18 U8 GPIO_SW_N
IO_L18P_18 AK7 GPIO_SW_E
IO_L18N_18 AK6 DVI_RESET_B
IO_L19P_18 V10 CPU_TRST
IO_L19N_18 V9 SPI_CE_B
VALUE
VCC0_EXP
EXP VCC0
U1
FF1136
BANK 13
W28 VCCO1_13
AB29 VCCO2_13
AA32 VCCO3_13
IO_L0P_SM8P_13 V32 HDR2_32_DIFF_3_P
IO_L0N_SM8N_13 V33 HDR2_30_DIFF_3_N
IO_L1P_SM7P_13 W34 HDR2_36_SM_15_P
IO_L1N_SM7N_13 V34 HDR2_34_SM_15_N
IO_L2P_SM6P_13 Y33 HDR2_40_SM_6_P
IO_L2N_SM6N_13 AA33 HDR2_38_SM_6_N
IO_L3P_SM5P_13 AA34 HDR1_26
IO_L3N_SM5N_13 V34 HDR1_30
IO_L4P_13 V32 HDR1_32
IO_L4N_VREF_13 W32 HDR1_34
IO_L5P_SM4P_13 AC34 HDR2_52_SM_5_P
IO_L5N_SM4N_13 AD34 HDR2_50_SM_5_N
IO_L6P_SM3P_13 AC32 HDR2_56_SM_13_P
IO_L6N_SM3N_13 AB32 HDR2_54_SM_13_N
IO_L7P_SM2P_13 AC33 HDR2_60_SM_4_P
IO_L7N_SM2N_13 AB33 HDR2_58_SM_4_N
IO_L8P_CC_SM1P_13 AF33 HDR2_48_SM_12_P
IO_L8N_CC_SM1N_13 AE33 HDR2_46_SM_12_N
IO_L9P_CC_SM0P_13 AF34 HDR2_44_SM_14_(CC)
IO_L9N_CC_SM0N_13 AE34 HDR2_42_SM_14_(CC)
IO_L10P_CC_13 AH34 HDR1_36
IO_L10N_CC_13 AJ34 HDR1_58(CC)
IO_L11P_CC_13 AD32 HDR1_28(CC)
IO_L11N_CC_13 AE32 HDR1_38(CC)
IO_L12P_VRN_13 AG33 FPGA_VRN_B13
IO_L12N_VRP_13 AH33 FPGA_VRP_B13
IO_L13P_13 AK34 HDR1_44
IO_L13N_13 AK33 HDR1_46
IO_L14P_13 AG32 HDR1_40
IO_L14N_VREF_13 AH32 HDR1_42
IO_L15P_13 AJ32 HDR1_48
IO_L15N_13 AK32 HDR1_50
IO_L16P_13 AL34 HDR1_52
IO_L16N_13 AL33 HDR1_54
IO_L17P_13 AM33 HDR1_56
IO_L17N_13 AM32 HDR1_60
IO_L18P_13 AN34 HDR1_62
IO_L18N_13 AN33 HDR1_64
IO_L19P_13 AN32 HDR2_64_SM_9_P
IO_L19N_13 AP32 HDR2_62_SM_9_N
VCCO_EXP
R22 49.9 1%
R23 49.9 1%
VALUE
VCC3V3
3.3V VCC0
U1
FF1136
BANK 20
J8 VCCO1_20
E10 VCCO2_20
H11 VCCO3_20
IO_L0P_20 E9 FPGA_CPU_RESET_B
IO_L0N_20 E8 GPIO_LED_C
IO_L1P_20 F9 IIC_SCL_MAIN
IO_L1N_20 F8 IIC_SDA_MAIN
IO_L2P_20 F10 FPGA_SERIAL2_TX
IO_L2N_20 G10 FPGA_SERIAL2_RX
IO_L3P_20 G8 SRAM_CLK
IO_L3N_20 H8 SRAM_ADV_LD_B
IO_L4P_20 D11 SRAM_BW1
IO_L4N_VREF_20 D10 SRAM_BW0
IO_L5P_20 K11 SRAM_BW3
IO_L5N_20 J11 SRAM_BW2
IO_L6P_20 D12 SRAM_DQP0
IO_L6N_20 C12 SRAM_DQP1
IO_L7P_20 H10 SRAM_DQP2
IO_L7N_20 H9 SRAM_DQP3
IO_L8P_CC_20 A13 SRAM_MODE
IO_L8N_CC_20 B12 SRAM_OE_B
IO_L9P_CC_20 J10 SRAM_CS_B
IO_L9N_CC_20 J9 SRAM_D31
IO_L10P_CC_20 K8 SRAM_D30
IO_L10N_CC_20 K9 SRAM_D29
IO_L11P_CC_20 B13 SRAM_D28
IO_L11N_CC_20 C13 SRAM_D27
IO_L12P_VRN_20 L10 FPGA_VRN_B20
IO_L12N_VRP_20 L11 FPGA_VRP_B20
IO_L13P_20 G11 SRAM_D26
IO_L13N_20 G12 SRAM_D25
IO_L14P_20 M8 SRAM_D24
IO_L14N_VREF_20 L8 SRAM_D23
IO_L15P_20 F11 SRAM_D22
IO_L15N_20 E11 SRAM_D21
IO_L16P_20 M10 SRAM_D20
IO_L16N_20 L9 SRAM_D19
IO_L17P_20 E12 SRAM_D18
IO_L17N_20 E13 SRAM_D17
IO_L18P_20 N10 SRAM_D16
IO_L18N_20 N9 FLASH_CLK
IO_L19P_20 F13 FLASH_ADV_B
IO_L19N_20 G13 FLASH_WAIT
VCC3V3
R26 49.9 1%
R27 49.9 1%
VALUE
Banks 11,12,13
Sys ACE, XGI,
PHY, LCD
XILINX
Title: Banks 11,12,13 Sys ACE, XGI, PHY, LCD
SCHEM, ROHS COMPLIANT
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415
0381241
Date: 1-22-2008_14:51
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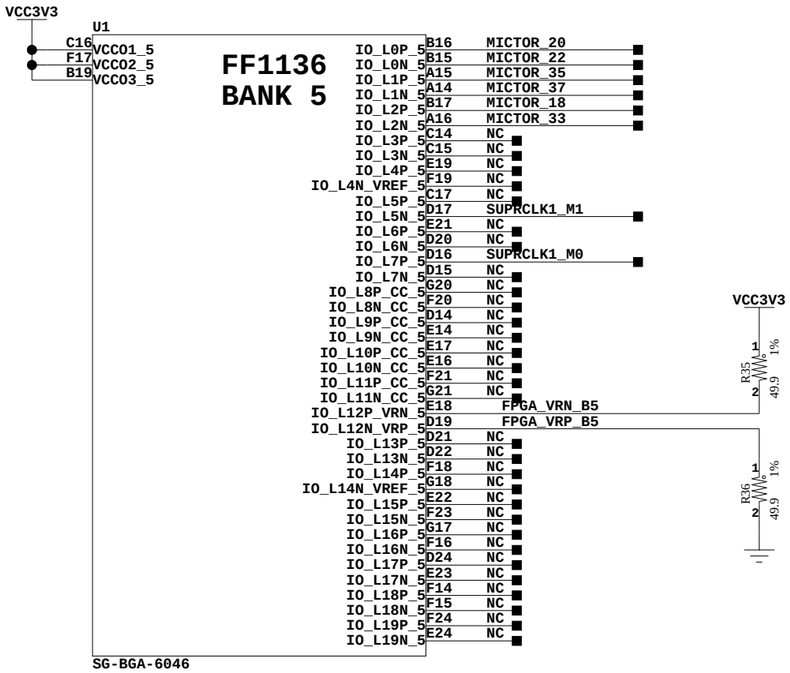
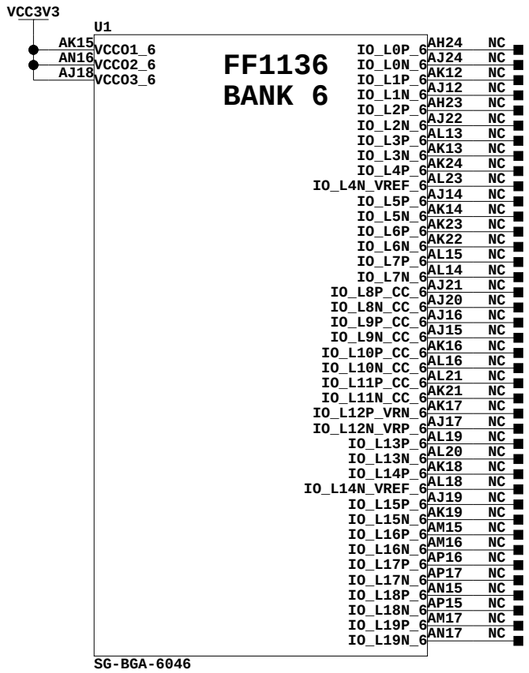
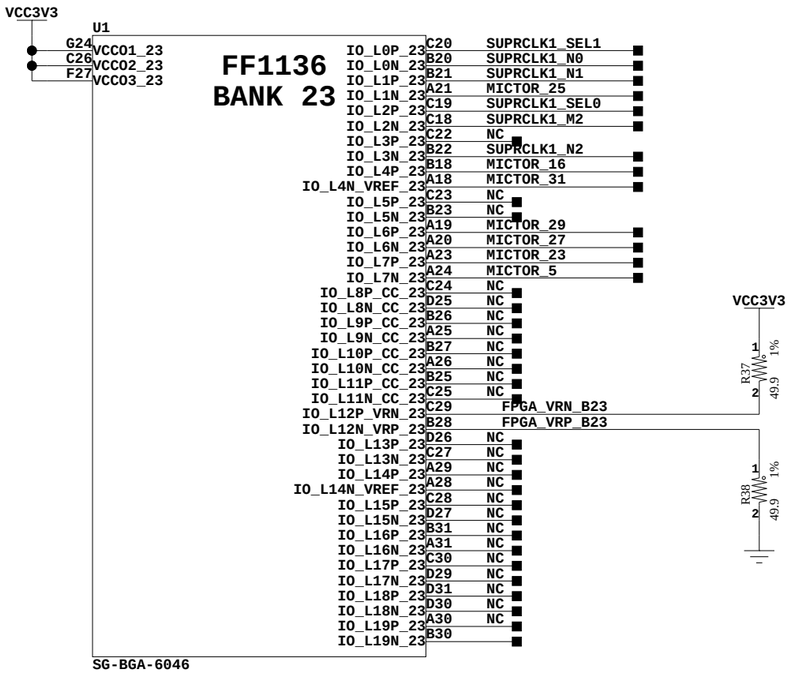
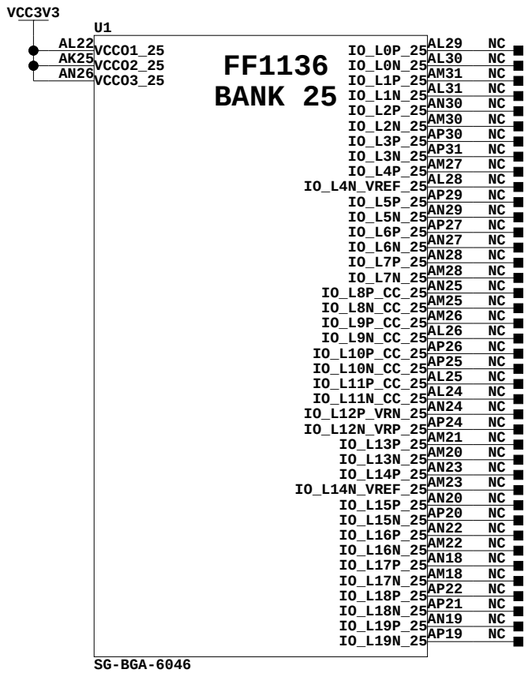
BP

Unused banks on the LX50T and SX50T









Banks 15, 17
VGA, IIC, PHY
SRAM, FLASH, GPIO

XILINX

Title:	Banks 11,12,13 VGA, IIC, PHY, SRAM, GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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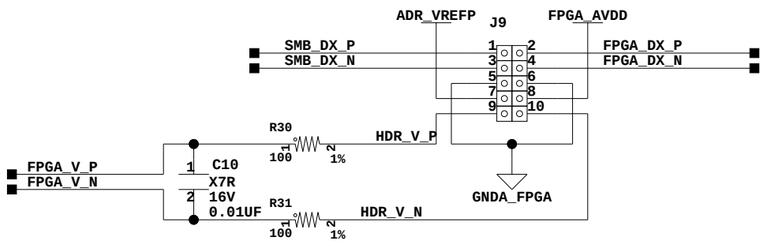
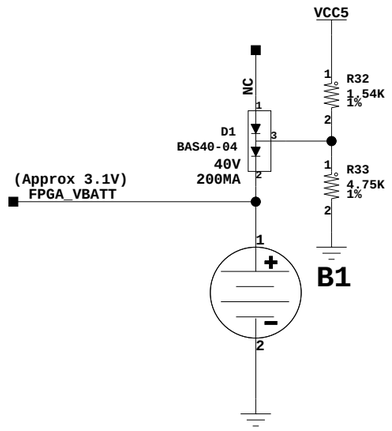
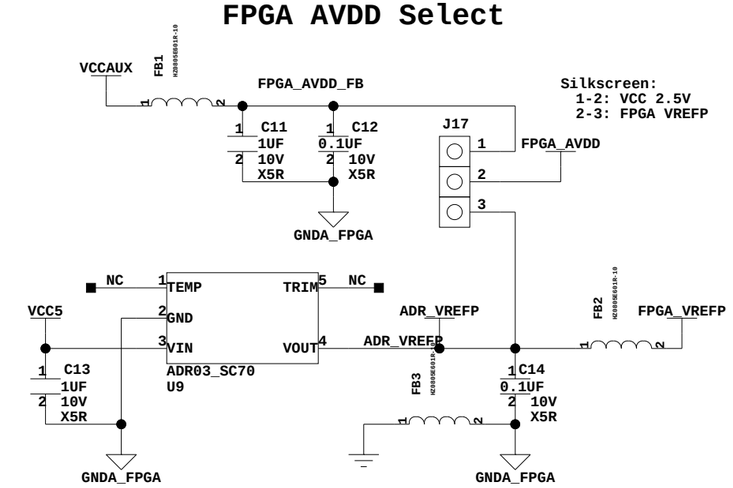
System Monitor Header

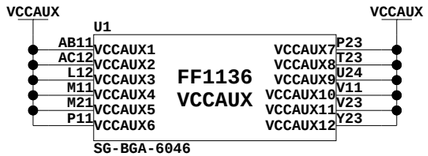


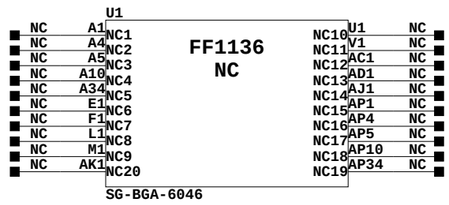
Rechargeable Battery

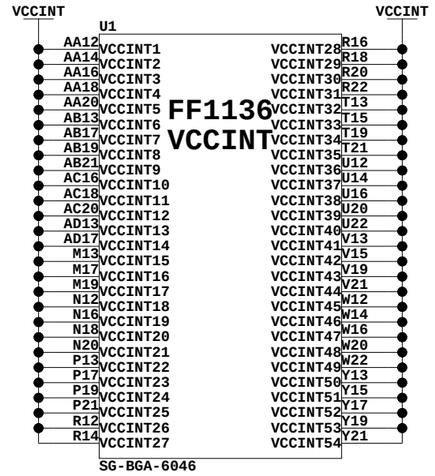


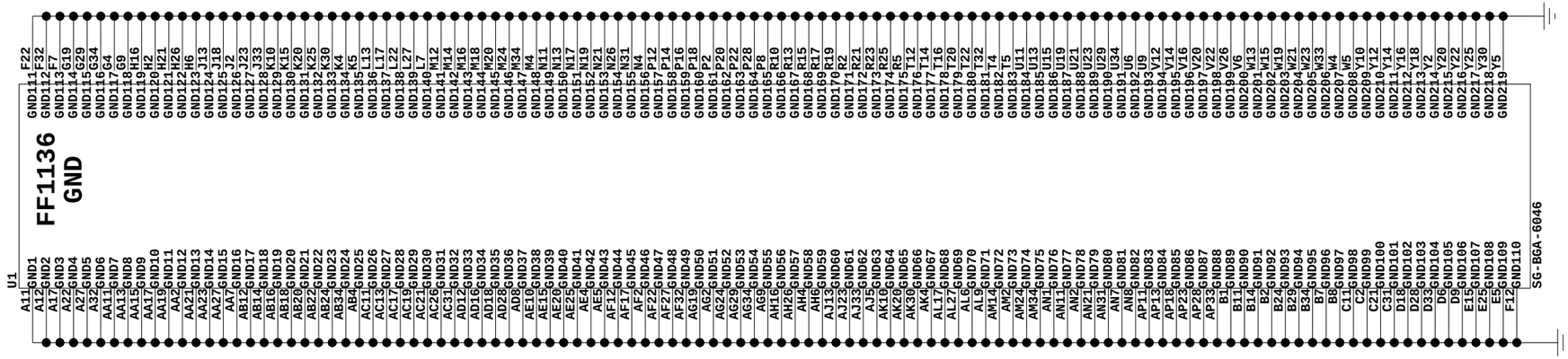
FPGA AVDD Select











Power and Misc FPGA Banks VCCINT, VCCAUX, NCs, GND Battery and System Moniter

XILINX

Title:	FPGA Misc, VCCINT, VCCAUX, GND, Sys Mon SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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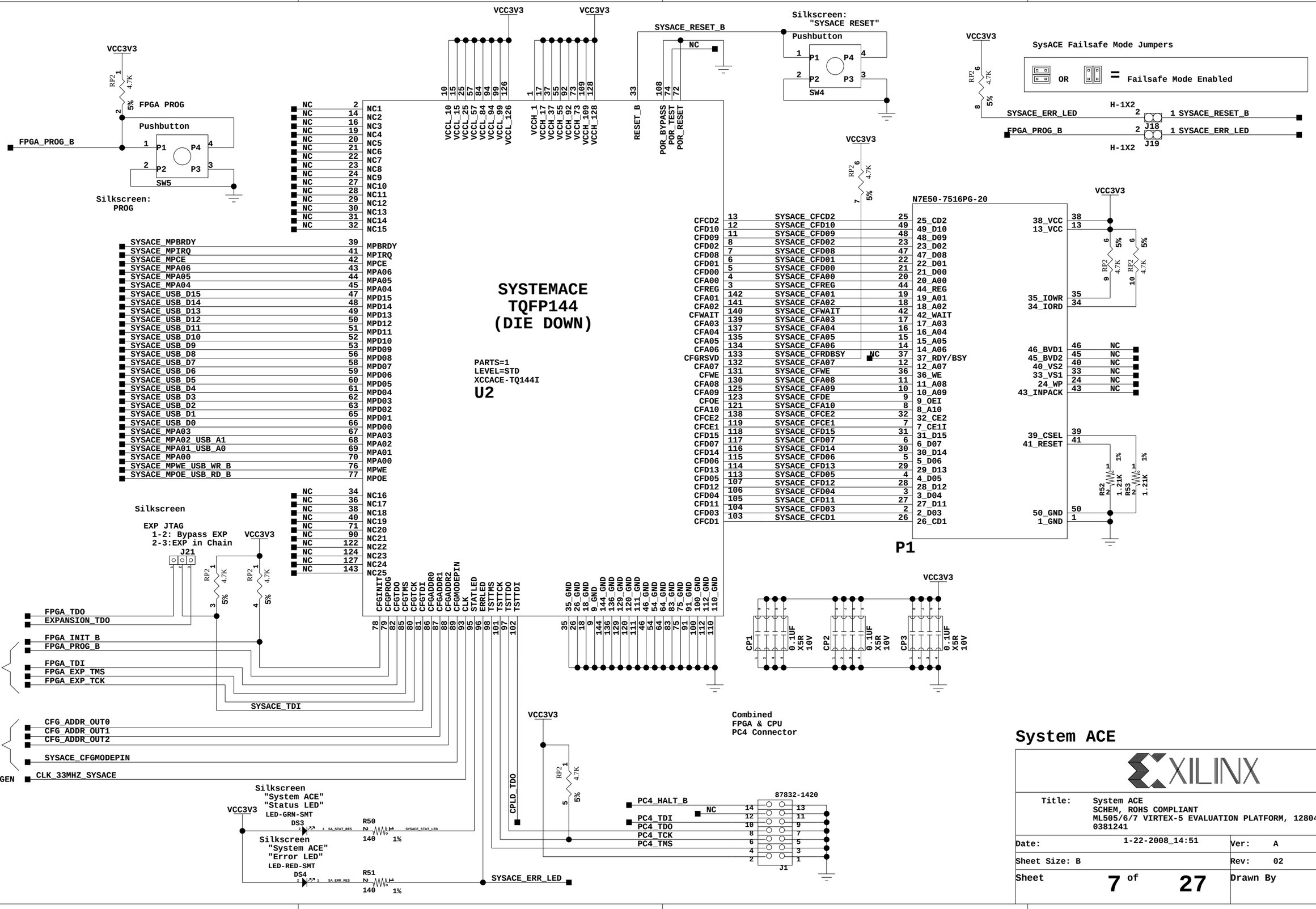

System ACE

Title:	System ACE SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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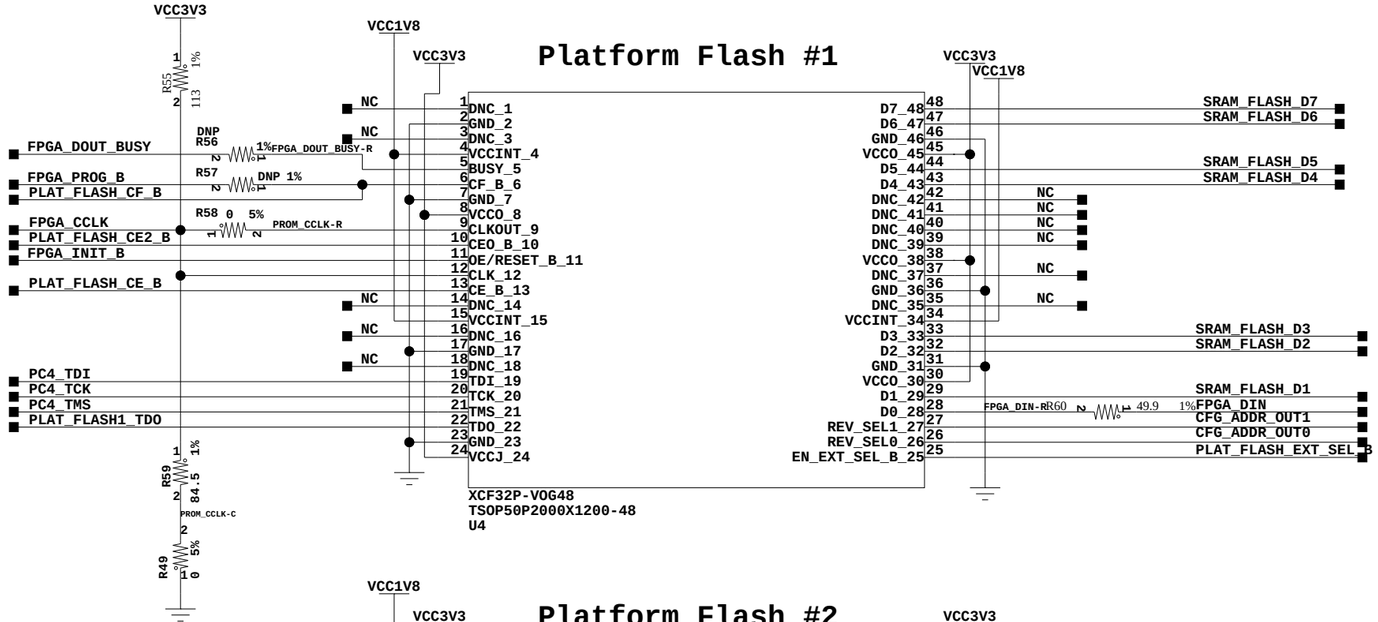
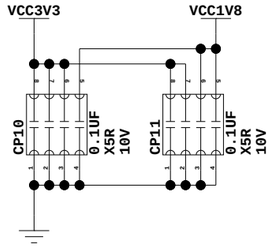
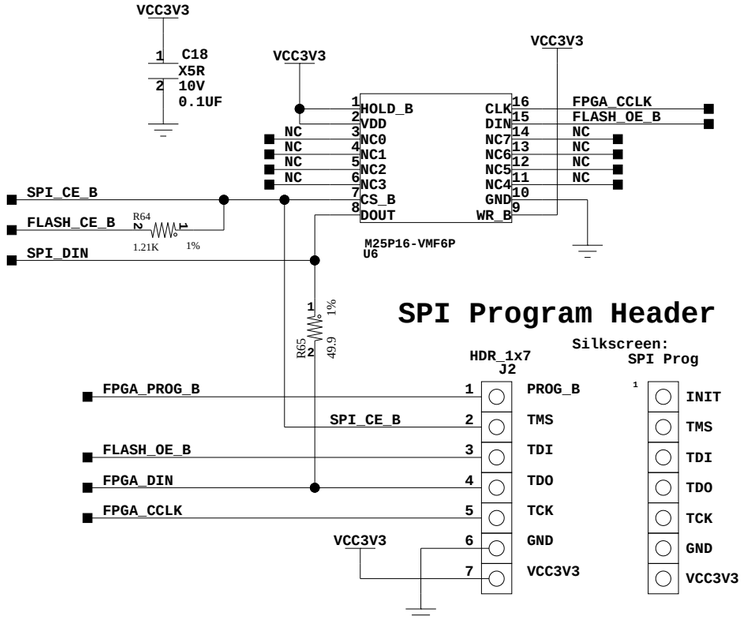
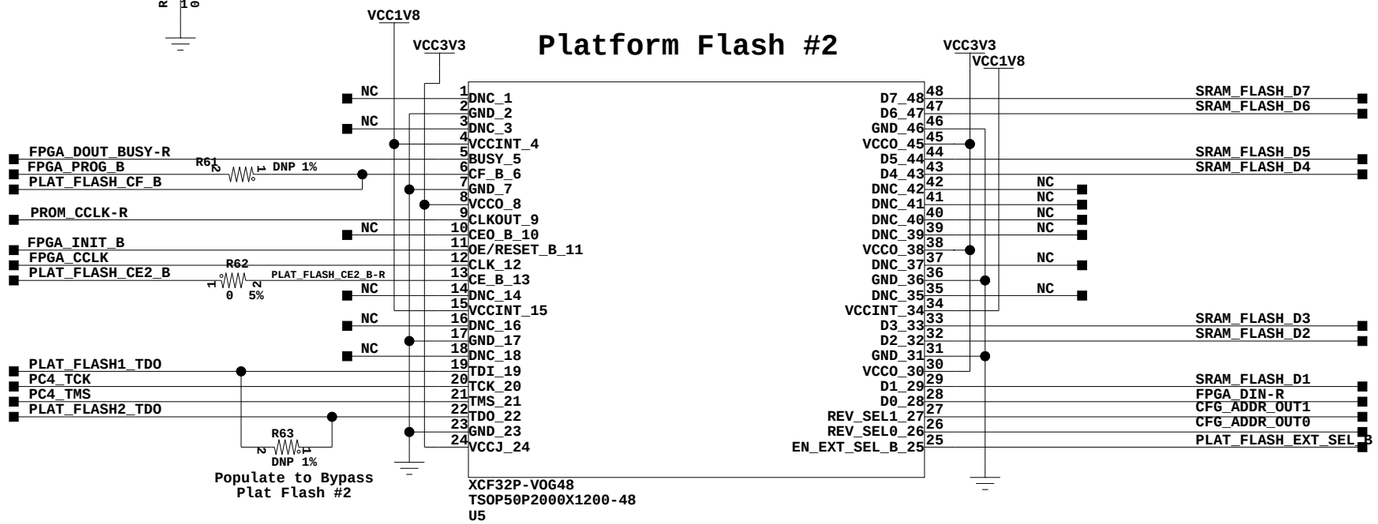
Platform Flash #1

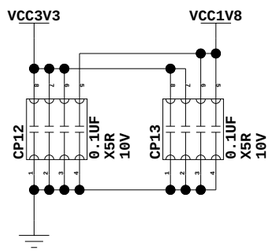




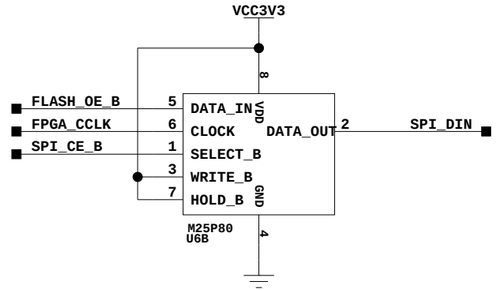


Platform Flash #2

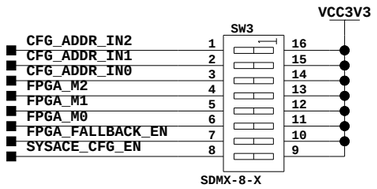




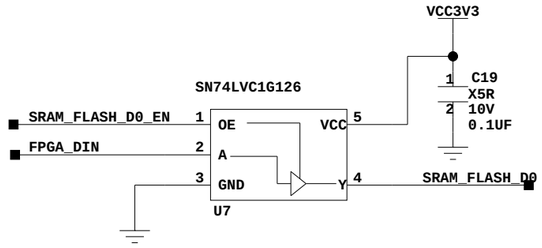
SPI Flash



Silkscreen:
SysACE Config, Mode pins



Config DIP switches



Toggles connection from Plat Flash D0 to SRAM D0

Misc Config
Platform Flash,
SPI Flash

XILINX

Title:	Misc Config,Platform Flash, SPI Flash SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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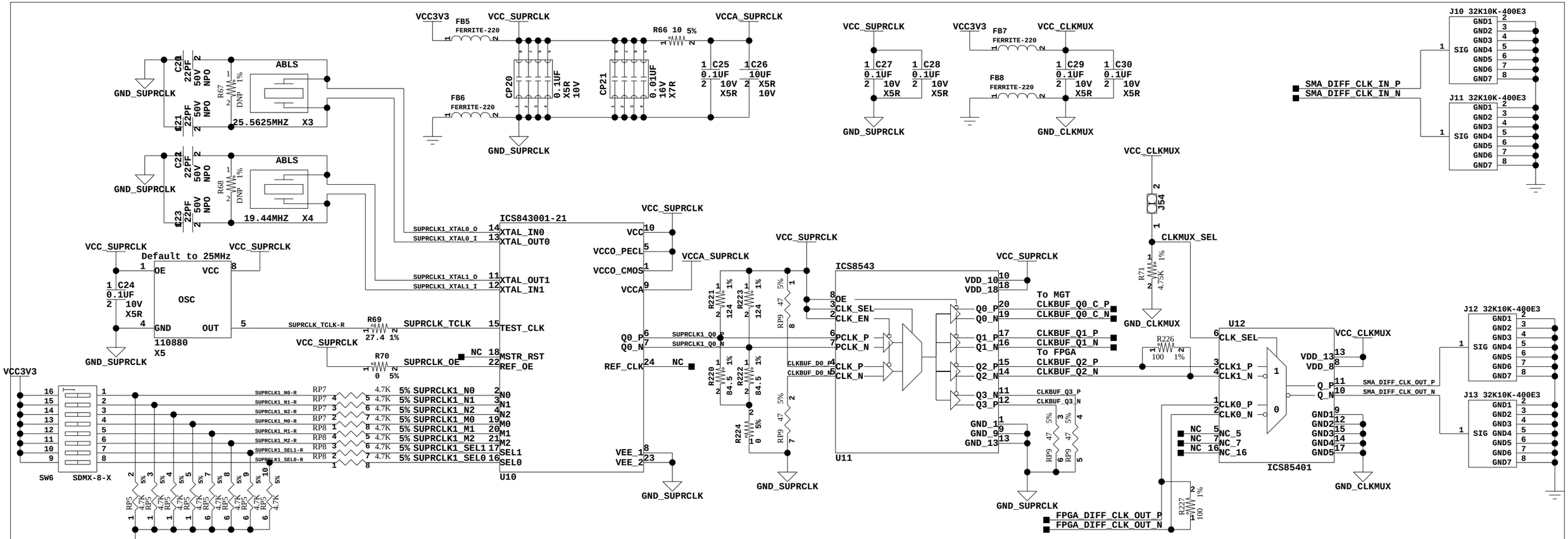
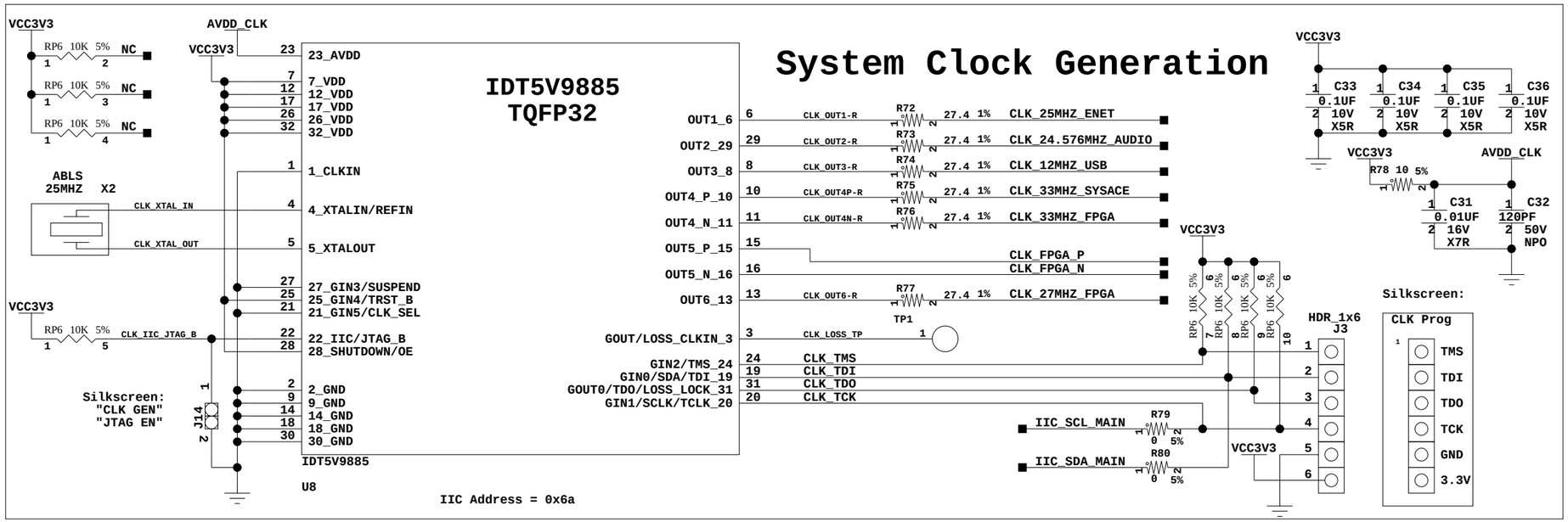
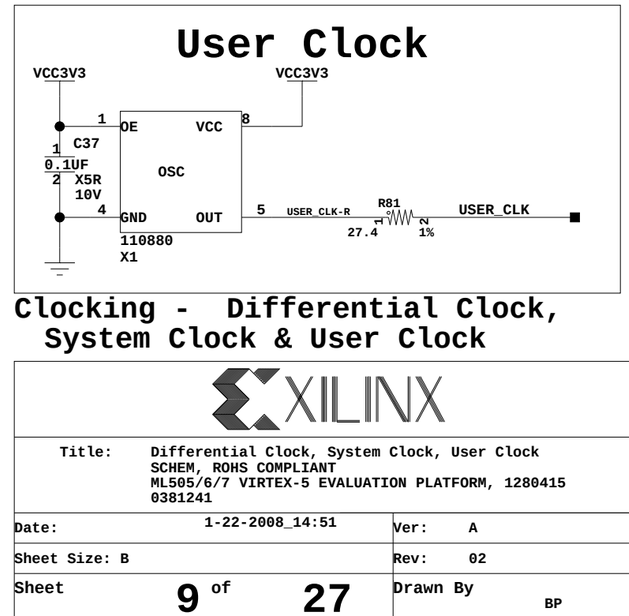
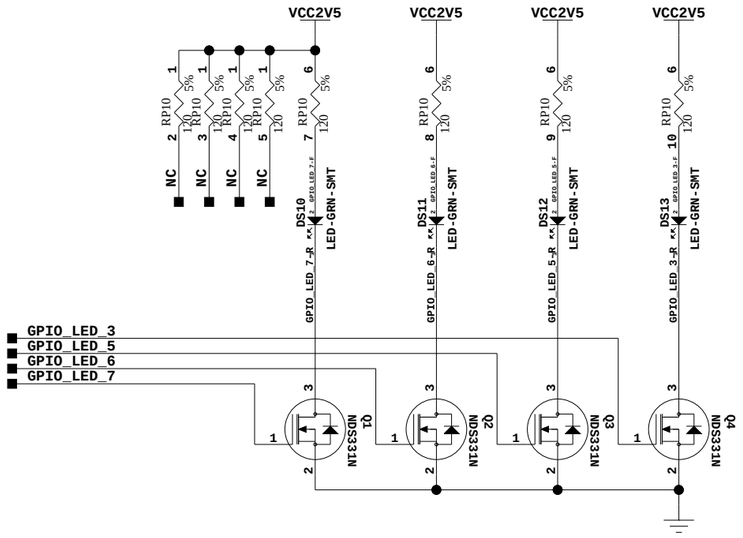
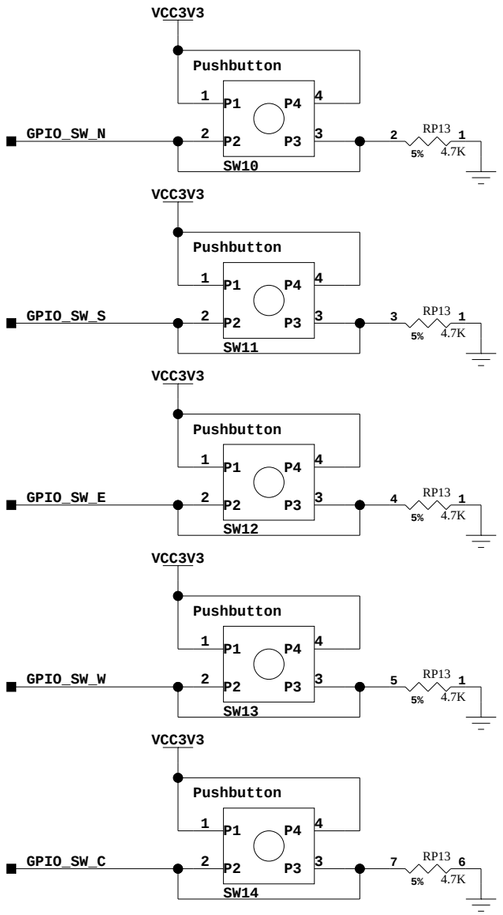
Diff Clocks: SMAs, Generation, MUX and Buffer

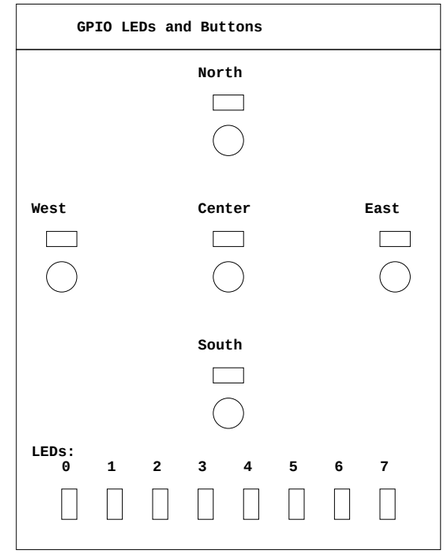


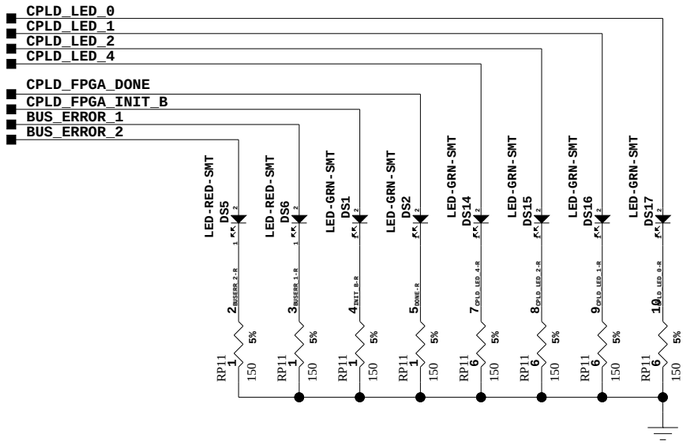


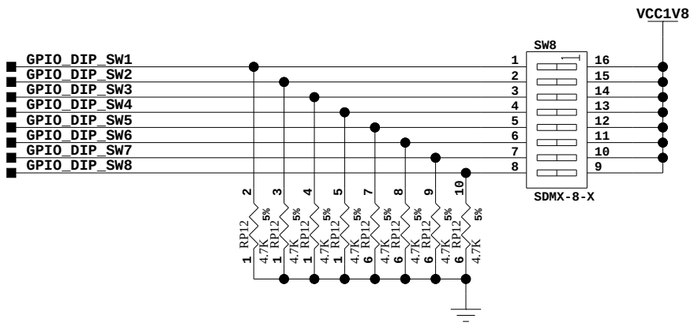


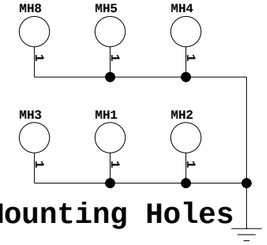




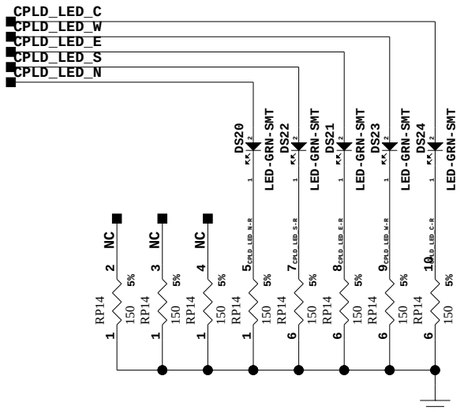




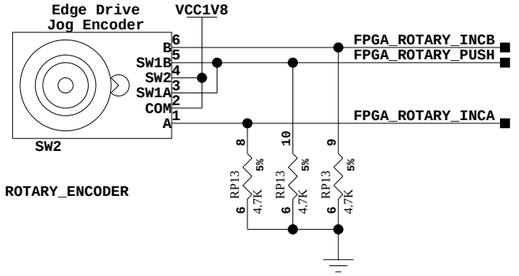


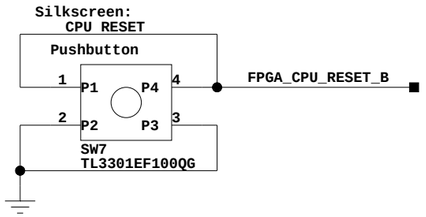


Mounting Holes



Edge Drive Jog Encoder Switch





GPIO - Buttons, LEDs, Switches

Title:	GPIO Buttons, LEDs, Switches GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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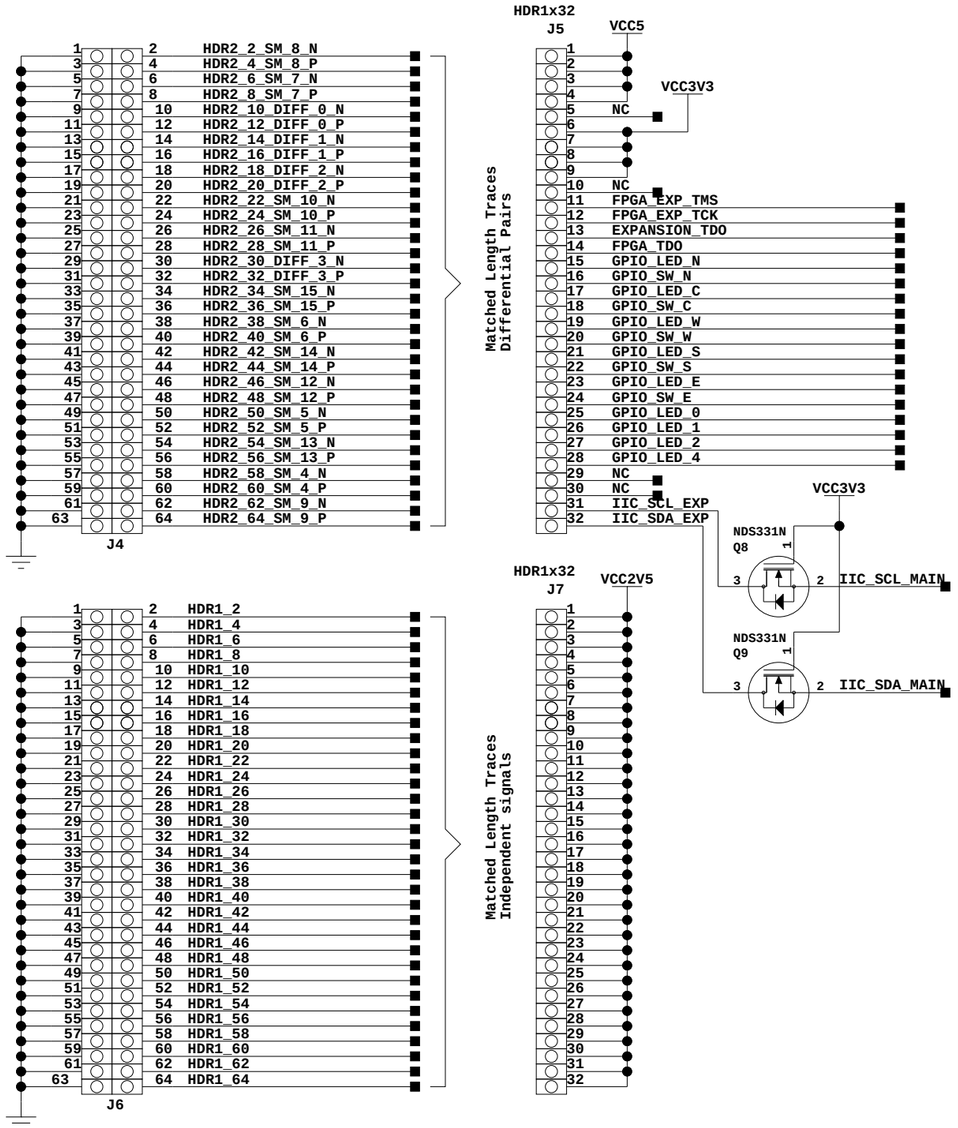
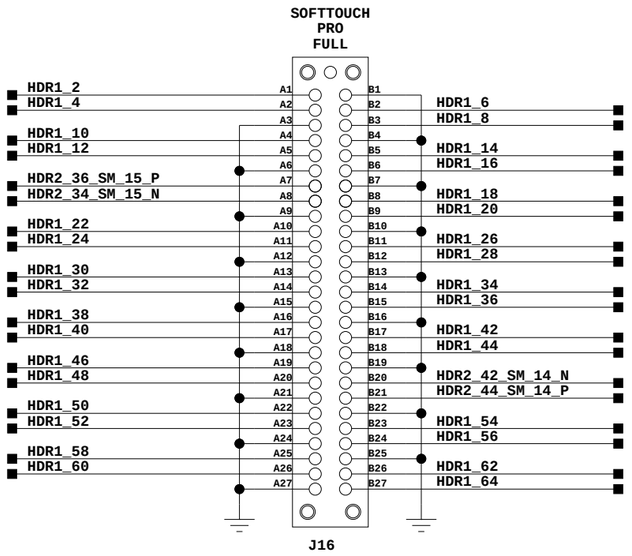
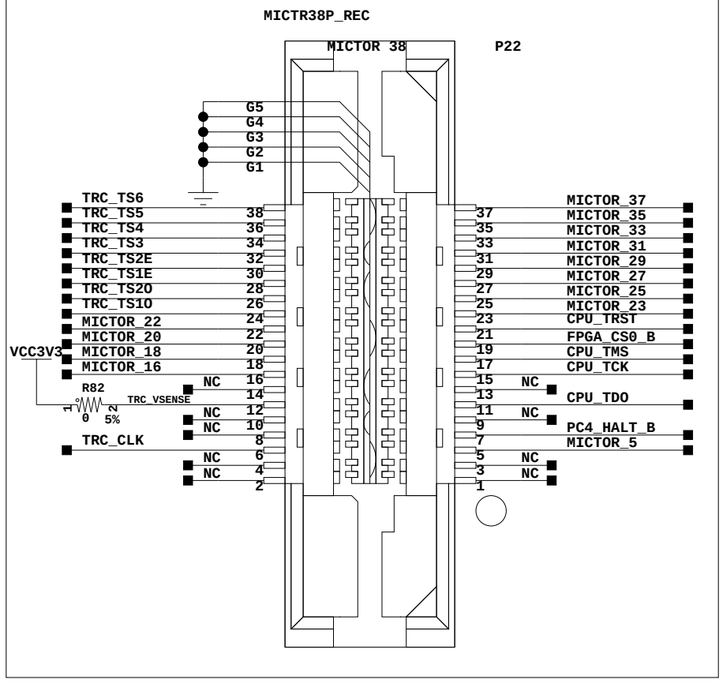
XGI Expansion Interface



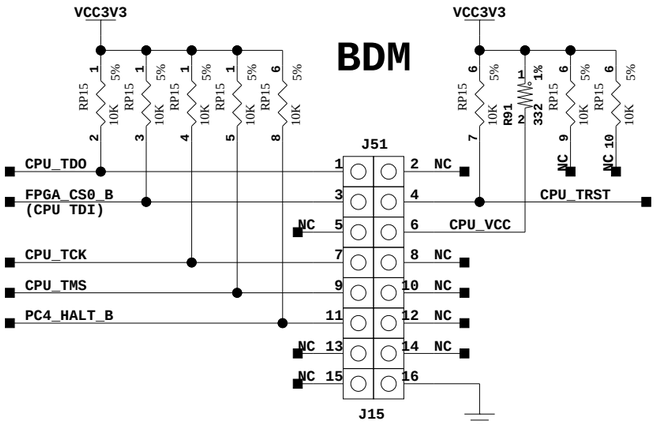
SoftTouch Pro



Mictor



BDM



XGI - Expansion Connector

Title:	XGI - Expansion Headers SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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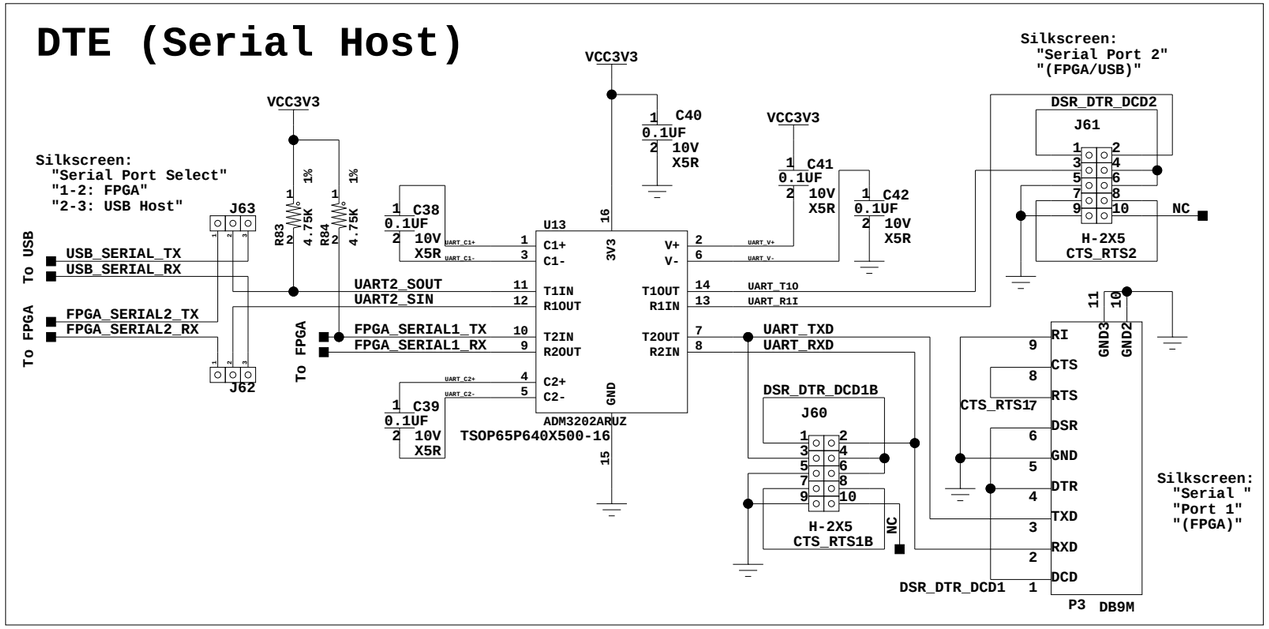
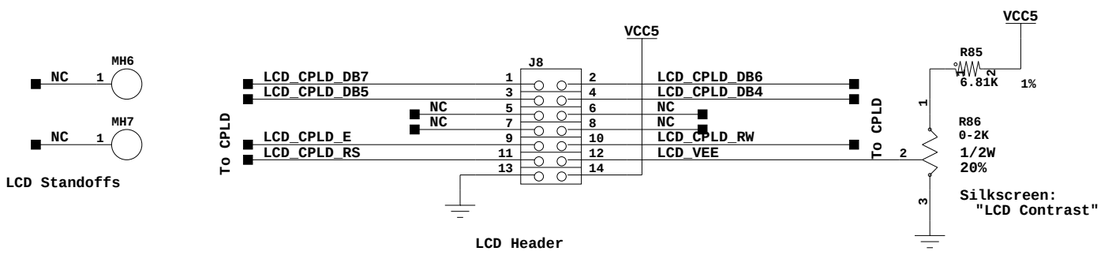
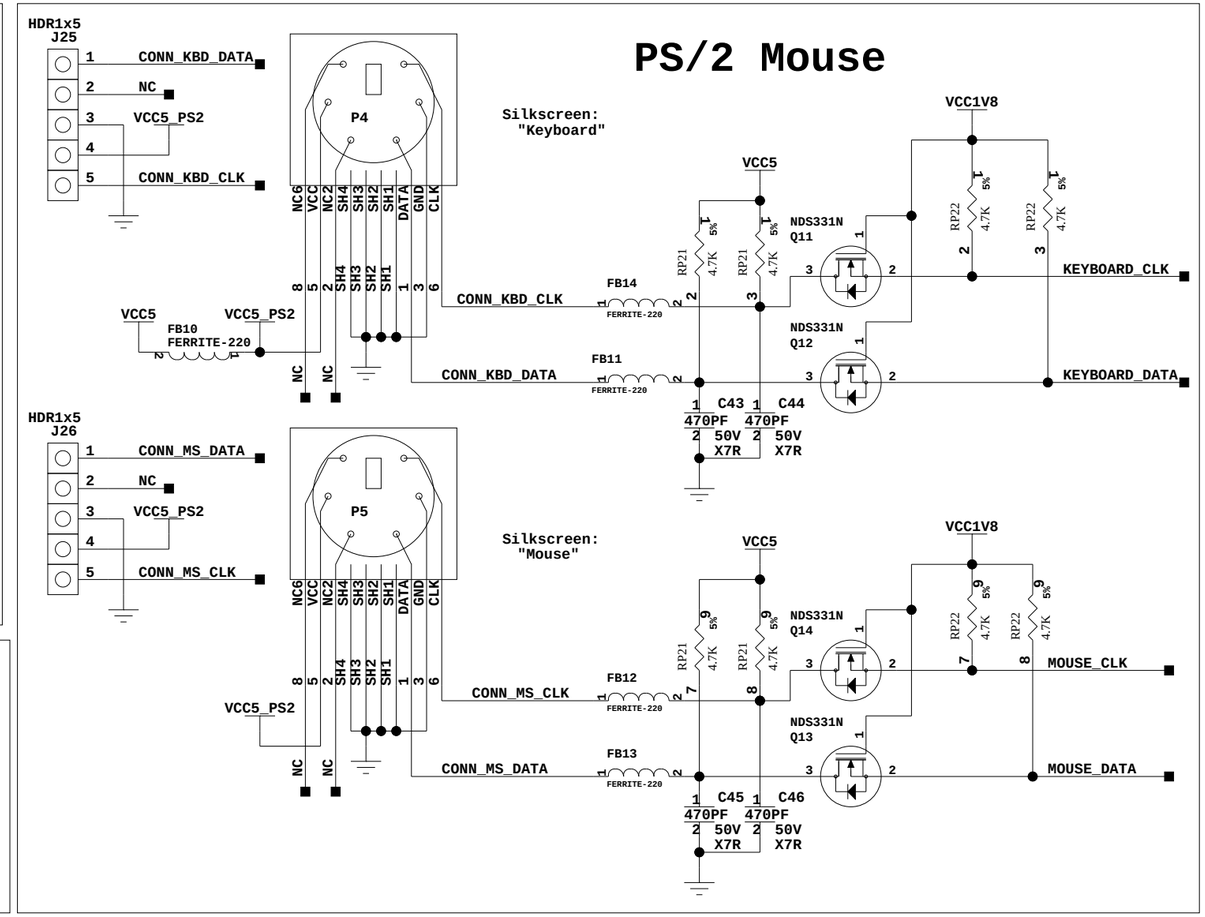
DTE (Serial Host)

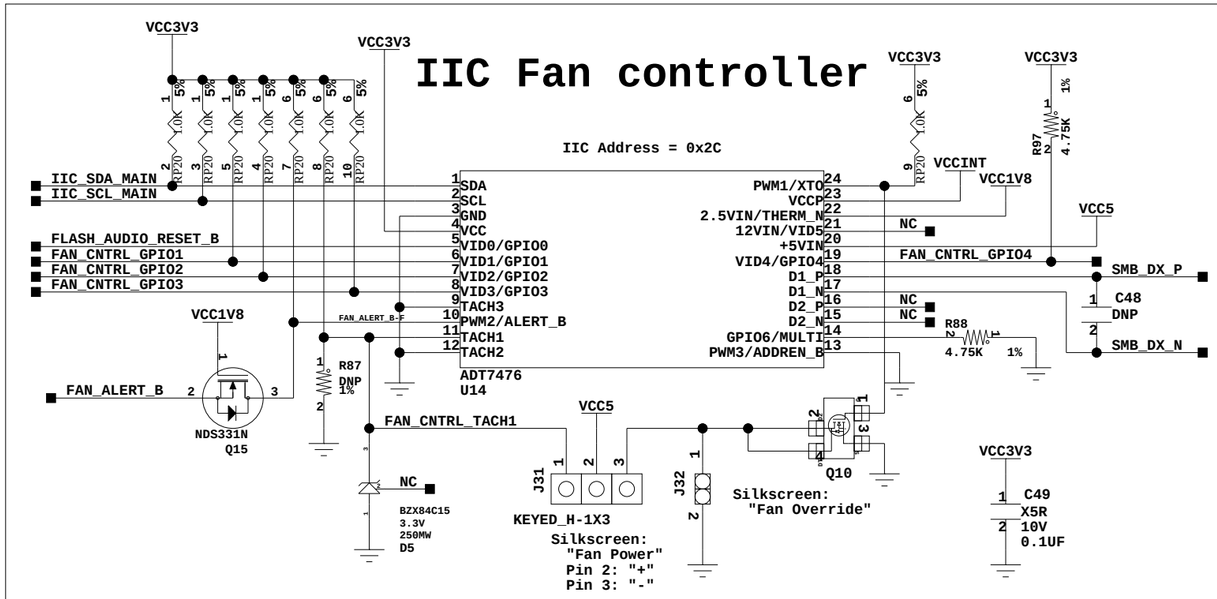




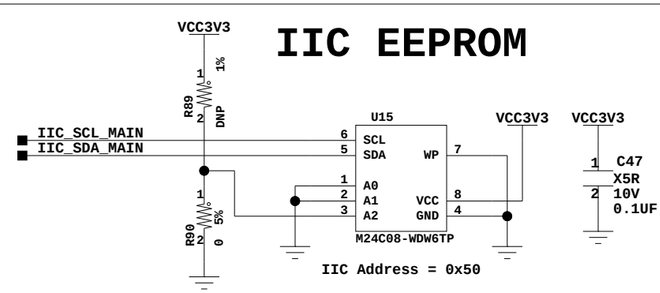
PS/2 Mouse

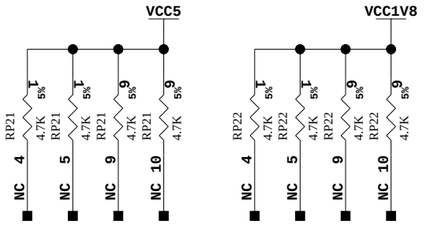


IIC Fan controller



IIC EEPROM





Misc - LCD, PS2, UART, Fan Controller

Title:	LCD, PS2, UART, IIC EEPROM, IIC Fan Controller SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:55	Ver:	A
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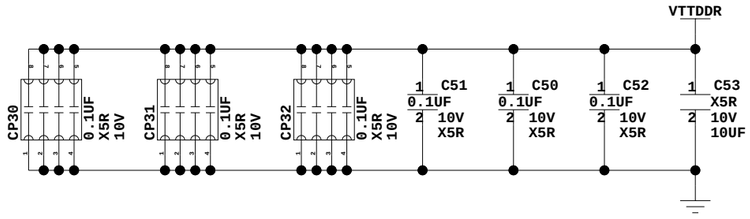

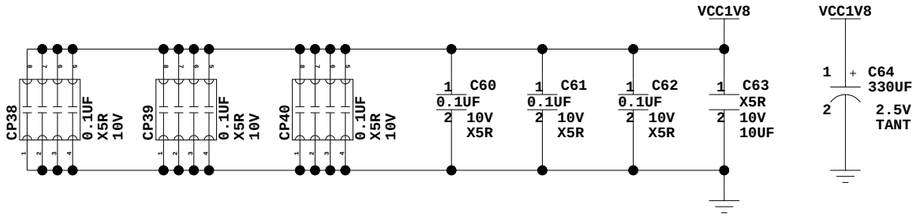

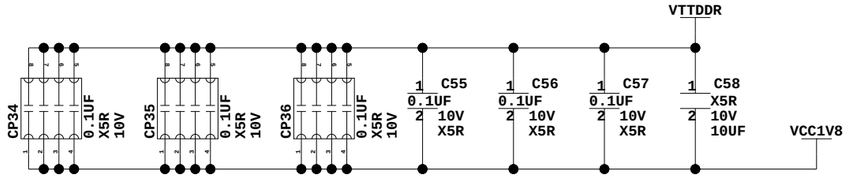

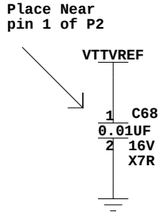

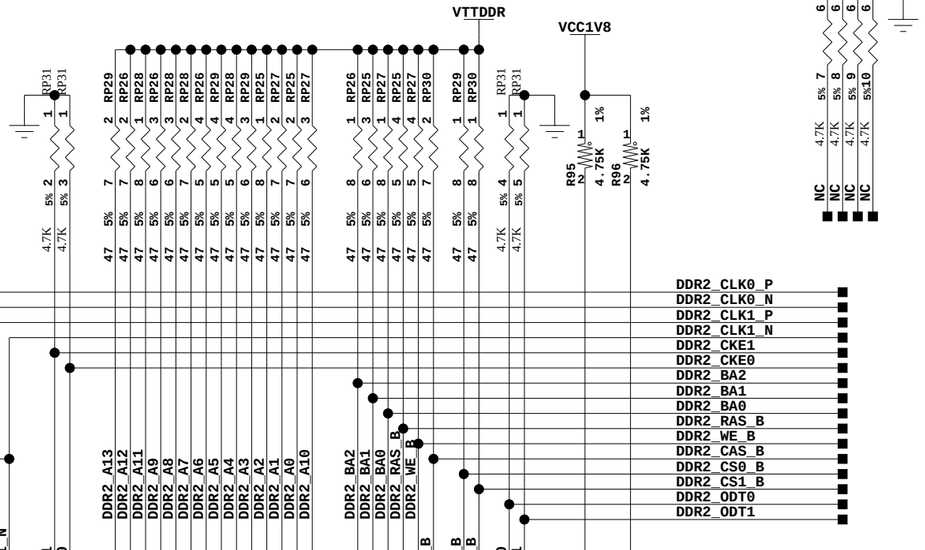

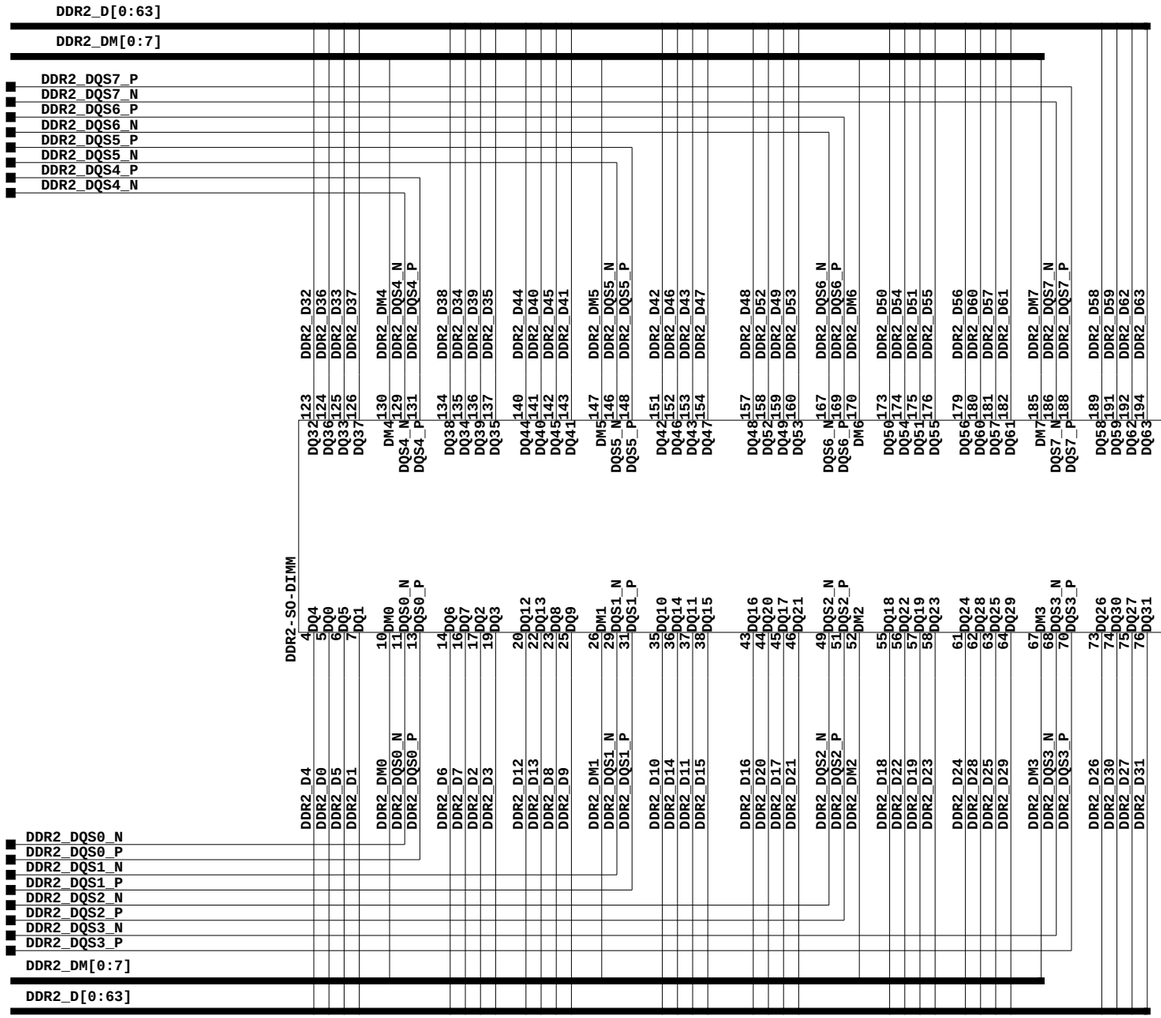

DDR2 SO-DIMM

XILINX

Title:	DDR2 SO-DIMM SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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The PHY MDIP Pins below are
Media Dependent Interface Pins (MDIP),
and are all bidirectional pins.

Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

J22, J23 pins 1-2: GMII/MII to Cu
J22, J23 pins 2-3: SGMII to Cu, no clk
J22 pins 1-2, J24 ON: RGMII, modified MII in Cu

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

10/100/1000 PHY

Title:	10/100/1000 PHY SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date:	1-22-2008_14:51
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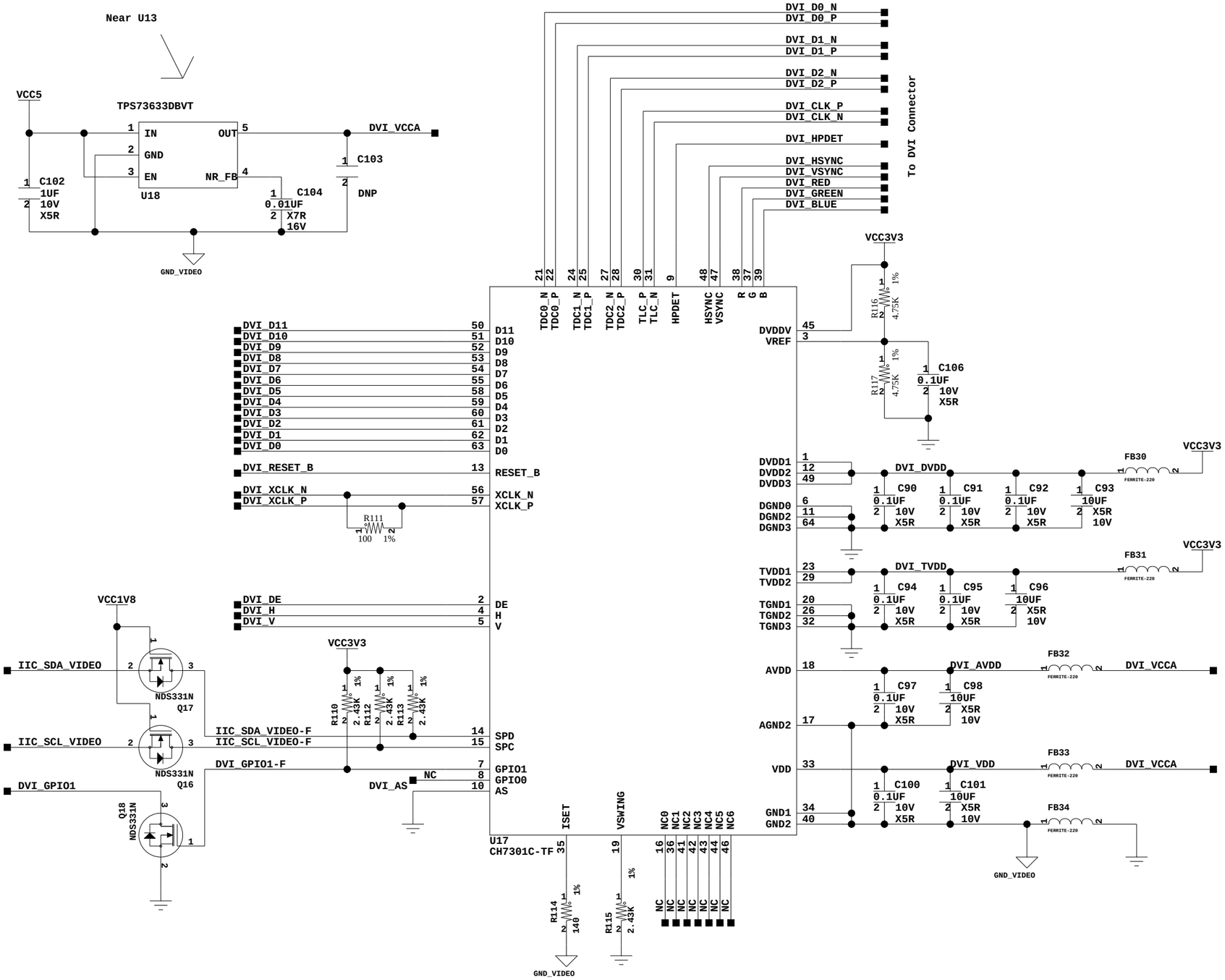

VGA Out Codec

Title:	VGA Out Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
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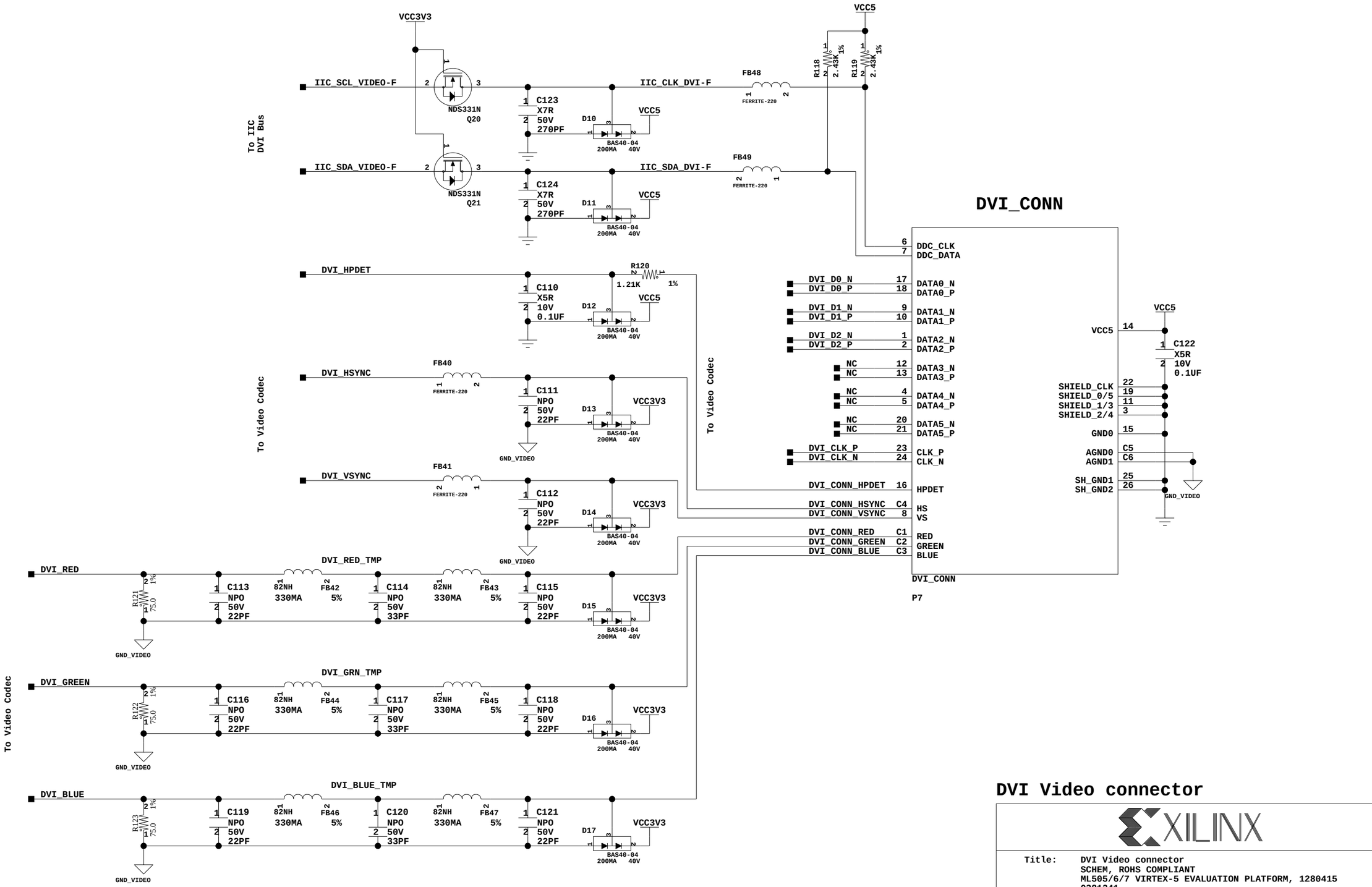

DVI Video connector

Title:	DVI Video connector SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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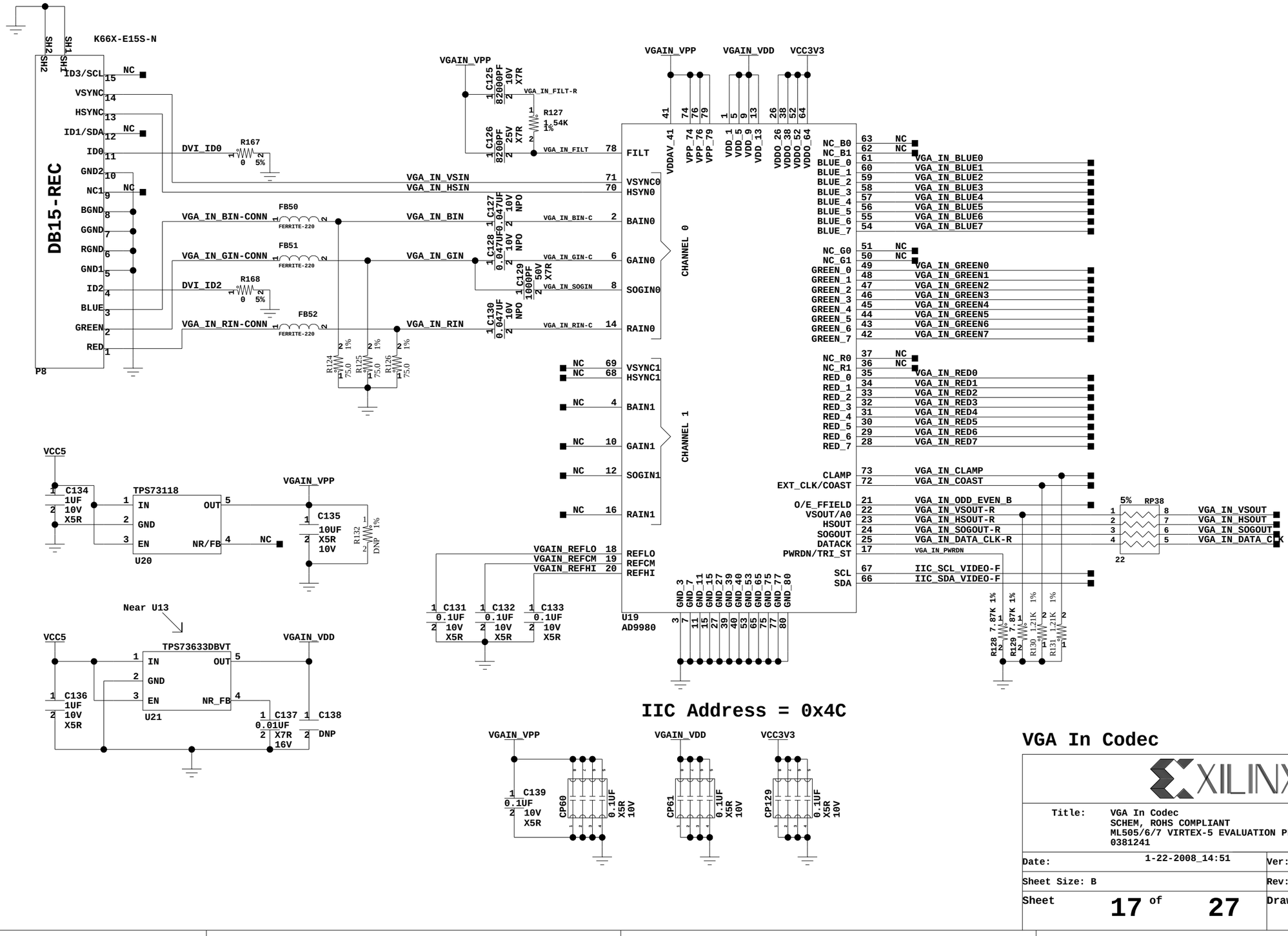

VGA In Codec

XILINX

Title:	VGA In Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date: 1-22-2008_14:51	Ver: A
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CLK_24.576MHZ_AUDIO
AUDIO_SDATA_OUT
AUDIO_BIT_CLK
AUDIO_SDATA_IN
AUDIO_SYNC
FLASH_AUDIO_RESET_B
PIEZO_SPEAKER

Portions of the design above this line are "Digital Ground", and should be outside the moat

Portions of the design below this line are "Analog Ground", and should be inside the moat

VCC3V3 SN74LVC1G126 VCC3V3
U45

R135 4.75K 1%
R136 4.75K 1%
R137 4.75K 1%
R138 4.75K 1%
R139 0 5%
R140 3.01K 1%
R141 3.01K 1%
R142 4.75K 1%
R143 4.75K 1%
R144 75.0 1%
R145 75.0 1%
R146 75.0 1%
R147 100 1%
R148 27.4 1%
R149 27.4 1%
R204 1.21K 1%
R205 1.21K 1%
R206 1.21K 1%
R157 4.75K 1%
R158 4.75K 1%

C140 1UF 10V X5R
C141 10UF X5R 10V
C142 1UF 10V X5R
C143 0.1UF 10V X5R
C144 0.1UF 10V X5R
C145 10UF X5R 10V
C146 0.1UF 10V X5R
C147 0.1UF 10V X5R
C148 0.1UF 10V X5R
C149 1UF 10V X5R
C150 0.1UF 10V X5R
C151 270PF 50V X7R
C152 270PF 50V X7R
C153 270PF 50V X7R
C154 270PF 50V X7R
C155 X5R 10V 0.1UF
C156 10UF X5R 10V
C157 1UF 10V X5R
C158 10V 0.1UFX5R
C159 10V 0.1UFX5R
C160 10V 1UF X5R
C161 10V 1UF X5R
C162 150UF 10V TANT
C163 150UF 10V TANT
C164 X5R 10V 1UF
C165 X5R 10V 1UF
C166 0.1UF 10V X5R

SP1

VCC5
VCC5_AUDIO
VCC3V3

AUDIO_SPDIF
To CPLD and Back
CPLD_SPDIF_1
CPLD_SPDIF_2
CPLD_SPDIF_3
RCA_SPDIF

Silkscreen: "SPDIF Out"
P14
CON_RCA_TH
RCA_JACK

Silkscreen: "Microphone In"
STEREO_JACK_TH
MIC2_CONN
MIC1_CONN
P10

STEREO_JACK_TH
P11
Silkscreen: "Line In"

AUDIO_PHONE
AUDIO_VREF_OUT
MIC1_IC
MIC2_IC
LINE_IN_L_IC
LINE_IN_R_IC
LINE_OUT_R_IC
LINE_OUT_L_IC

NC
PC_NC
RESET_N_11
SYNC_10
DVDD2_9
SDATA_IN_8
DVSS2_7
BIT_CLK_6
SDATA_OUT_5
DVSS1_4
XTL_OUT_3
XTL_IN_2
DVDD1_1

13_PHONE_IN
14_AUX_L
15_AUX_R
16_JS1
17_JS0
18_CD_L
19_CD_GND_REF
20_CD_R
21_MIC1
22_MIC2
23_LINE_IN_L
24_LINE_IN_R

25_AVDD1
26_AVSS1
27_VREF
28_VREFOUT
29_AFLT1
30_AFLT2
31_AFLT3
32_AFLT4
33_AVSS4
34_AVDD4
35_LINE_OUT_L
36_LINE_OUT_R

SPDIF_48
EAPD_47
ID1_N_46
ID0_N_45
AVSS3_44
AVDD3_43
NC_42
HP_OUT_R_41
AVSS2_40
HP_OUT_L_39
AVDD2_38
MONO_OUT_37

HP_OUT_R_IC
HP_OUT_L_IC

AD1981B
LQFP48

AC97
U22

FB55
FERRITE-220

RP41 4.7K

J28
H-2X5
MIC2_CONN
MIC1_CONN
LINE_OUT_R_CONN
LINE_OUT_L_CONN

HP_OUT_R_CONN
HP_OUT_L_CONN
LINE_OUT_R_CONN
LINE_OUT_L_CONN

STEREO_JACK_TH
P13
Silkscreen: "Amplified Line Out"
P12
Silkscreen: "Line Out"

Audio Codec

XILINX

Title:	Audio Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date: 1-22-2008_14:51	Ver: A
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Silkscreen:
"USB Peripheral 1"
USB_B_PERI_SMT
VCC
D_N
D_P
GND
USB_PERI1_VCC
USB_PERI1_D-
USB_PERI1_D+
R150 20.5K 1%
R151 49.9K 1%
C170 0.1UF 10V X5R
USB_GPIO25
P17
SH1
SH2
SH3
SH4
HDR1x5
J83
USB_HOST1_VCC
USB_HOST1_D-
USB_HOST1_D+
USB_HOST1_GND
Silkscreen:
"USB Host"
P18
FB60 FERRITE-220
FB61 FERRITE-220
C171 0.1UF 10V X5R
C178 0.1UF 10V X5R
VCC3V3
R152 4.75K 1%
R153 4.75K 1%
USB_GPIO29
USB_GPIO26
NC
MIC2025
U24
EN
FLG
GND
NC1
OUT2
IN
OUT1
NC2
VCC5
USB_HOST_VCC
C176 0.1UF 10V X5R
C177 150UF 10V TANT
USB Host Power
U23
CY7C67300-100AI
(DIE UP)
CYP_USB_HOST
USB_D0
USB_D1
USB_D2
USB_D3
USB_D4
USB_D5
USB_D6
USB_D7
USB_RESET_B
GND3_100
BEL_N_A0_99
BEH_N_98
A16_97
A18_96
A17_95
GPIO0_D0_94
GPIO1_D1_93
GPIO2_D2_92
GPIO3_D3_91
GPIO4_D4_90
GPIO5_D5_89
VCC2_88
GPIO6_D6_87
GPIO7_D7_86
RESET_N_85
RSVD_84
D0_83
D1_82
D2_81
D3_80
D4_79
D5_78
D6_77
D7_76
1_A1
2_A2
3_A3
4_DM2B
5_DP2B
6_AGND
7_A4
8_A5
9_DM2A
10_DP2A
11_OTGVBUS
12_CSWITCHB
13_CSWITCHA
14_VSWITCH
15_BOOSTGND
16_BOOSTVCC
17_A6
18_DM1B
19_DP1B
20_A7
21_AVCC
22_DM1A
23_DP1A
24_A8
25_A9
GND2_75
D8_MISO_74
D9_nSSI_73
D10_SCK_72
D11_MOSI_71
D12_TXD_70
D13_RXD_69
D14_RTS_68
D15_CTS_67
GPIO8_D8_MISO_66
GPIO9_D9_nSSI_65
WR_N_64
VCC0_63
RD_N_62
GPIO10_D10_SCK_61
GPIO11_D11_MOSI_60
GPIO12_D12_59
GPIO13_D13_58
GPIO14_D14_57
GPIO15_D15_SSI_N_56
GPIO16_A0_TXD_PWM0_55
GPIO17_A1_RXD__54
GPIO18_A2_RTS__53
GPIO19_A0_CS0_52
GND1_51
SYSACE_USB_D8
SYSACE_USB_D9
SYSACE_USB_D10
SYSACE_USB_D11
SYSACE_USB_D12
SYSACE_USB_D13
SYSACE_USB_D14
SYSACE_USB_D15
SYSACE_MPA01_USB_A0
GPIO_IRQ0
26_GND0
27_A10
28_XTALOUT
29_XTALIN
30_A11
31_A12
32_A13
33_A14
34_MEMSEL_N
35_ROMSEL_N
36_RAMSEL_N
37_VCC1
38_A15
39_GPIO31_SCK
40_GPIO30_SDA
41_GPIO29_OTGID
42_GPIO28_TX
43_GPIO27_RX
44_GPIO26_CTS_PWM3
45_GPIO25_IRQ1
46_GPIO24_INT_IORDY_IRQ0
47_GPIO23_RD_N_IOR
48_GPIO22_WR_N_IOW
49_GPIO21_CS_N
50_GPIO20_A1_CS1
CLK_12MHZ_USB
R156 49.9K 1%
IIC_SCL_USB
IIC_SDA_USB
USB_GPIO29
USB_SERIAL_TX
USB_SERIAL_RX
USB_GPIO26
USB_GPIO25
USB_INT
SYSACE_MPOE_USB_RD_B
SYSACE_MPWE_USB_WR_B
USB_CS_B
SYSACE_MPA02_USB_A1
C172 0.1UF 10V X5R
C173 0.1UF 10V X5R
C174 0.1UF 10V X5R
C175 0.1UF 10V X5R
Bypass cap for USB chip
R154 4.75K 1%
R155 4.75K 1%
"Abort Boot"
J33
U25
SCL
SDA
WP
A0
A1
A2
VCC
GND
M24128-BWDW6TP
SDA/SCL lines swapped for an
EEPROM larger than 16KB

USB Controller

XILINX

Title:	USB Controller SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date: 1-22-2008_14:51	Ver: A
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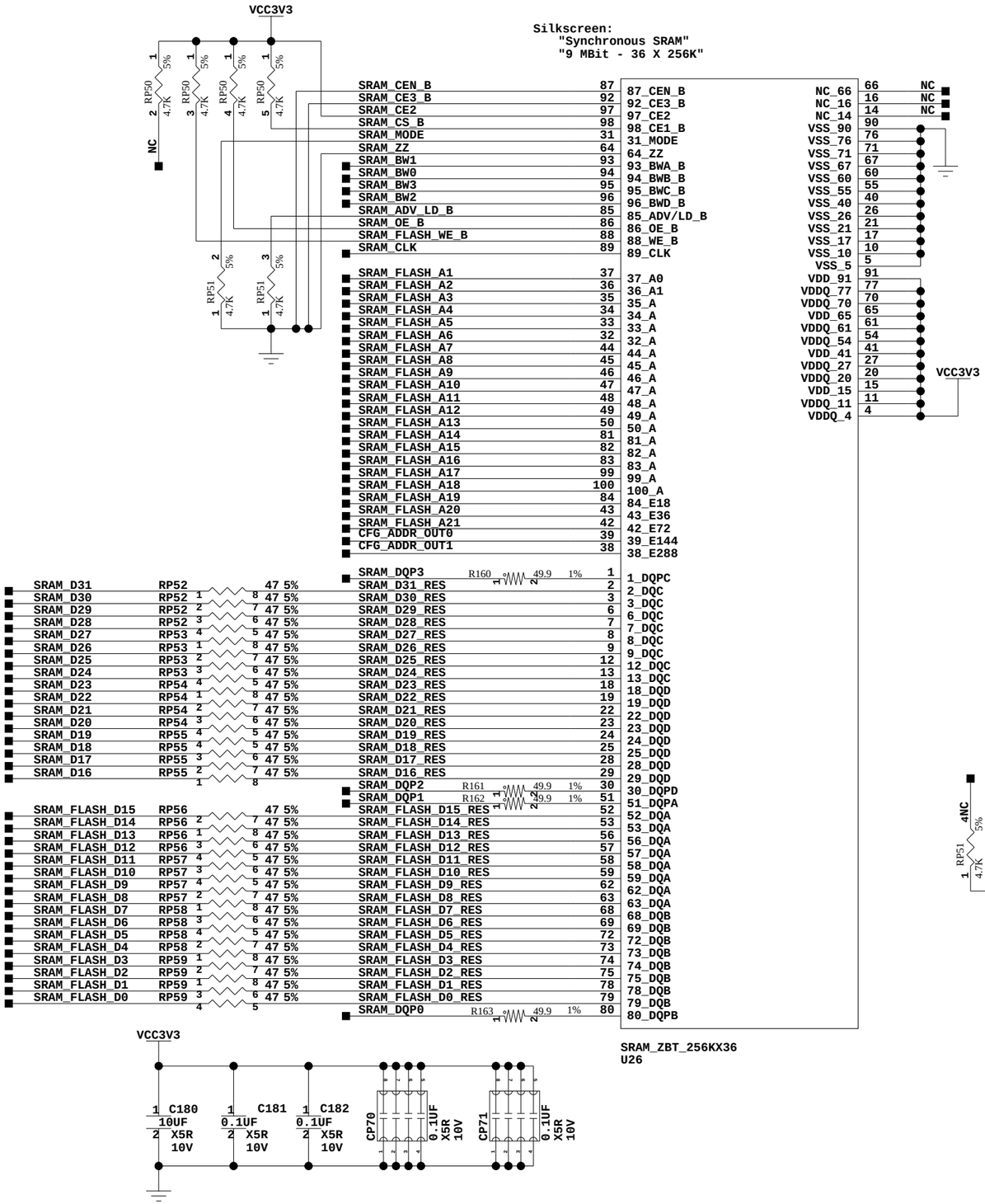
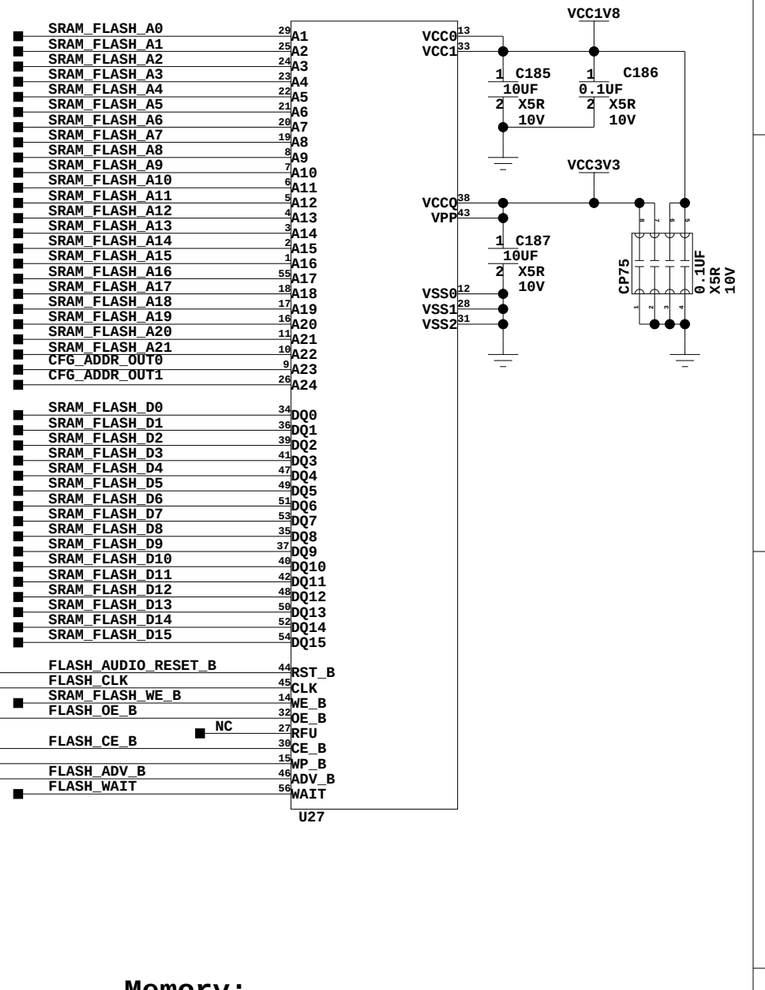
Sheet 19 of 27	Drawn By BP

The burst order mode of the SRAM is set to "Linear" by default

Silkscreen:
"Synchronous SRAM"
"9 MBit - 36 X 256K"



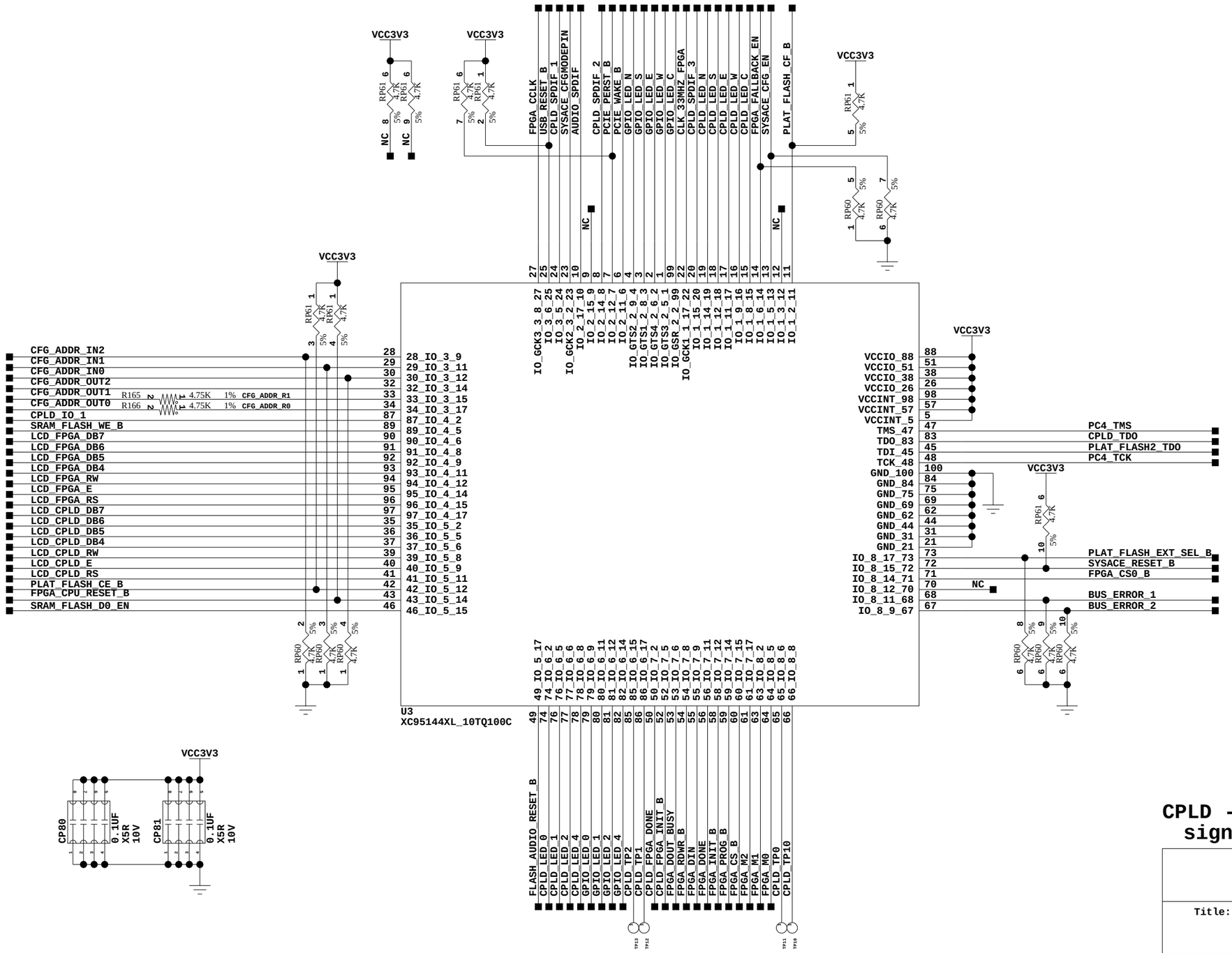
Silkscreen:
"Strata FLASH"
"256 MBit"



Memory:
Synchronous SRAM,
Strata FLASH

XILINX

Title:	Sync. SRAM, FLASH SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	20 of 27	Drawn By	BP



CPLD - Misc signal control

Title:	CPLD - Misc signal control SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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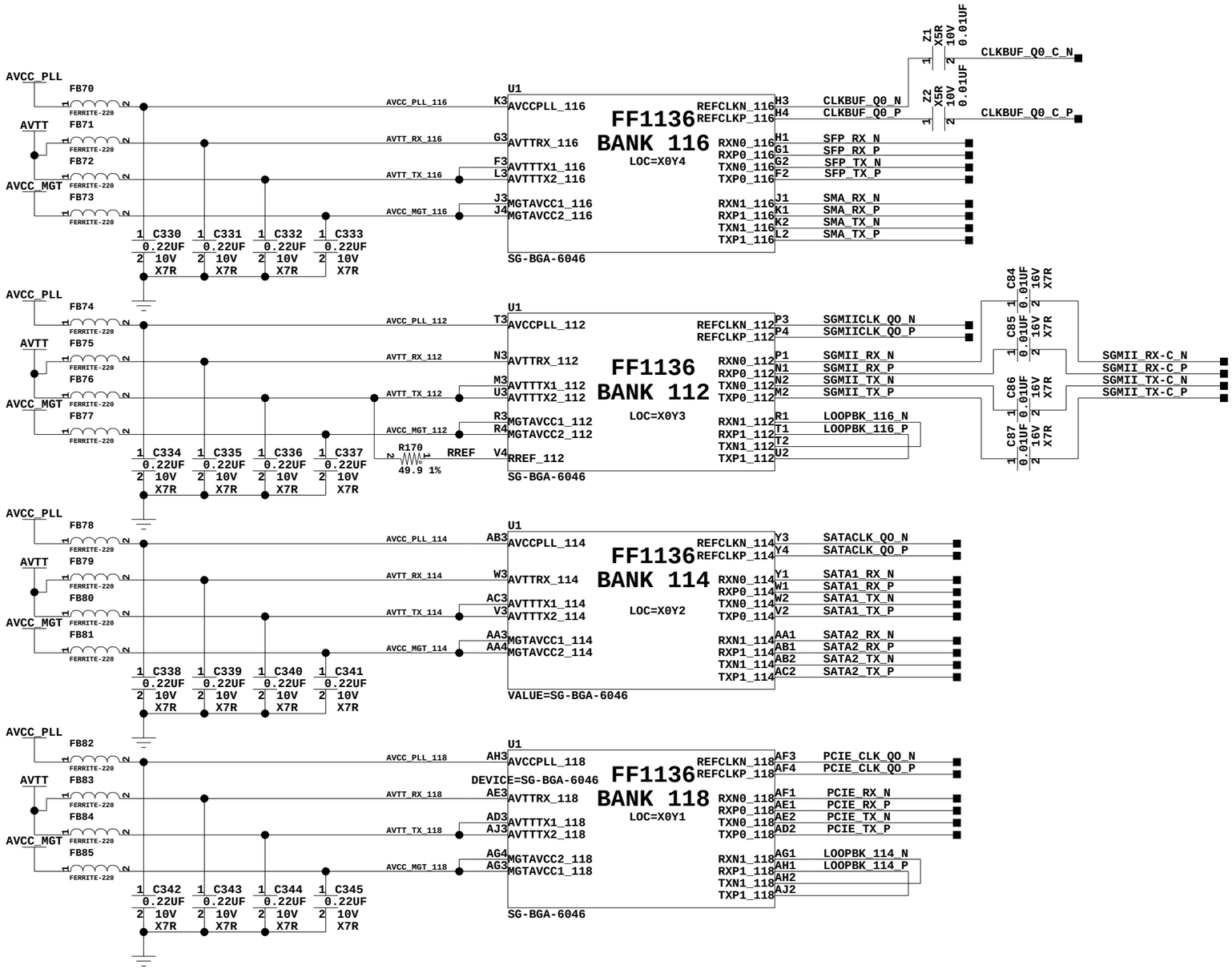

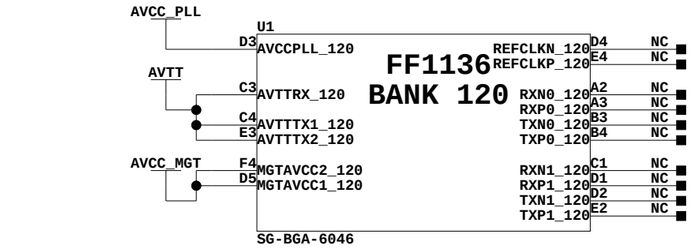

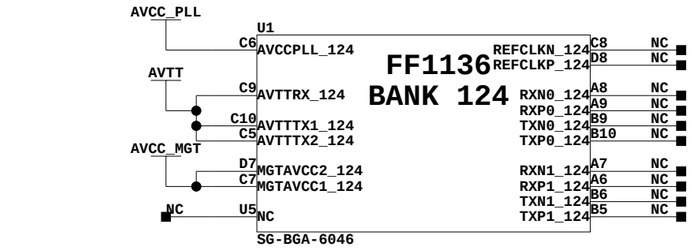

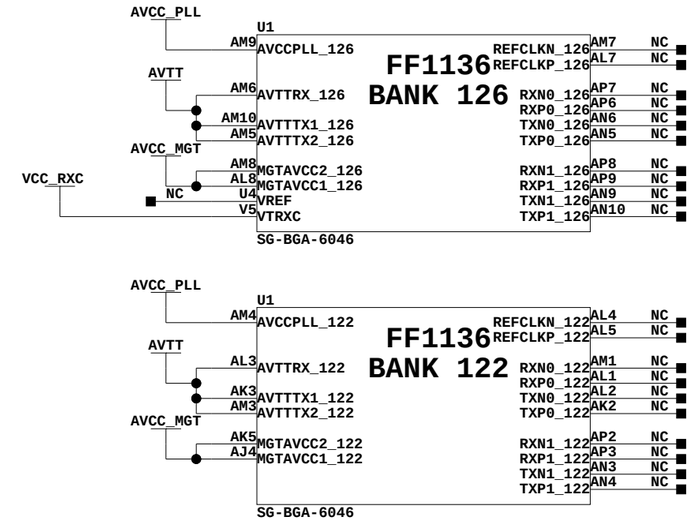

XILINX

Title:	MGT Banks SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:55	Ver:	A
Sheet Size: B		Rev:	02
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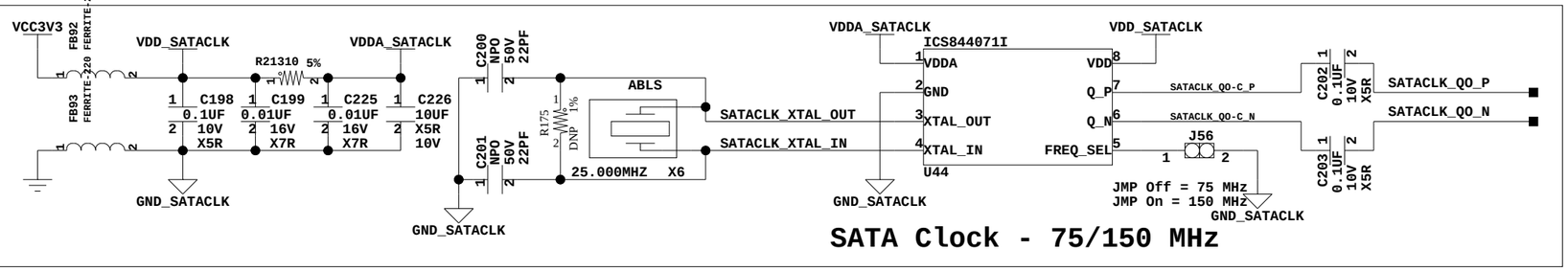
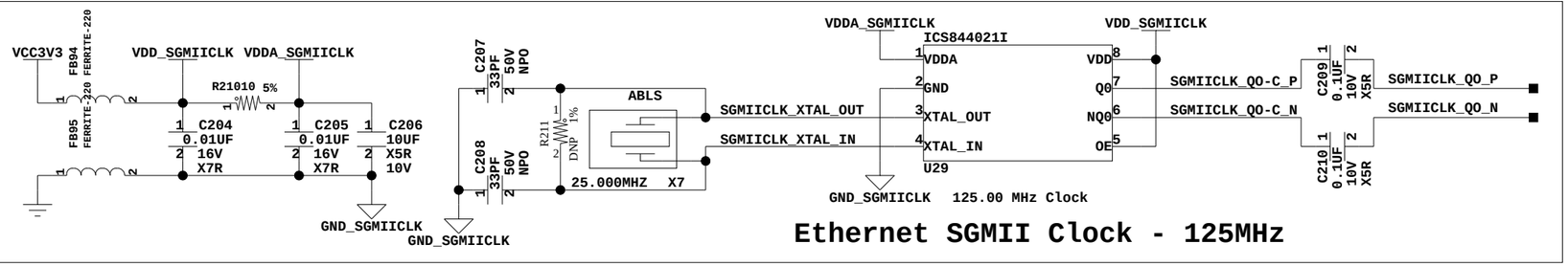
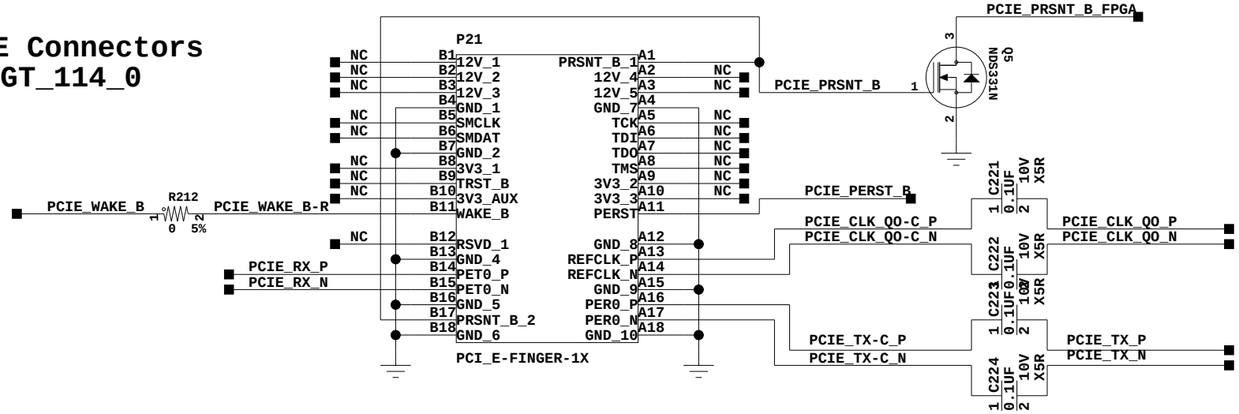


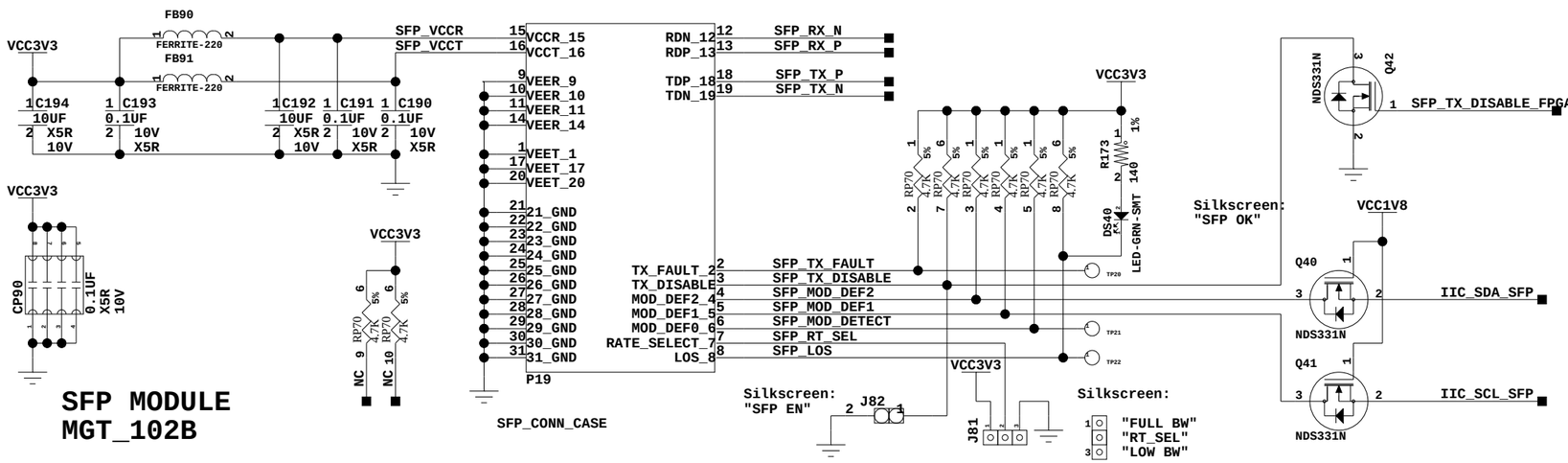
SATA Clock - 75/150 MHz



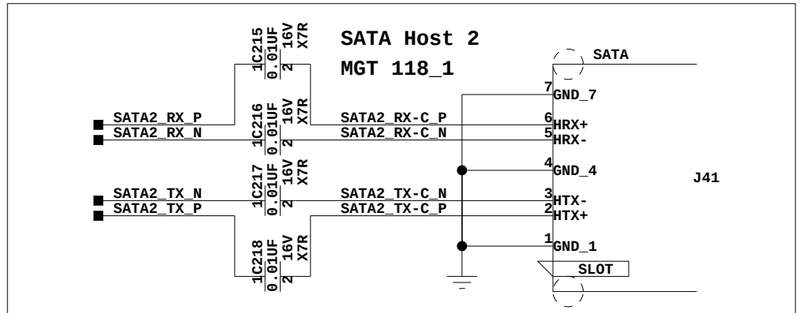
Ethernet SGMII Clock - 125MHz

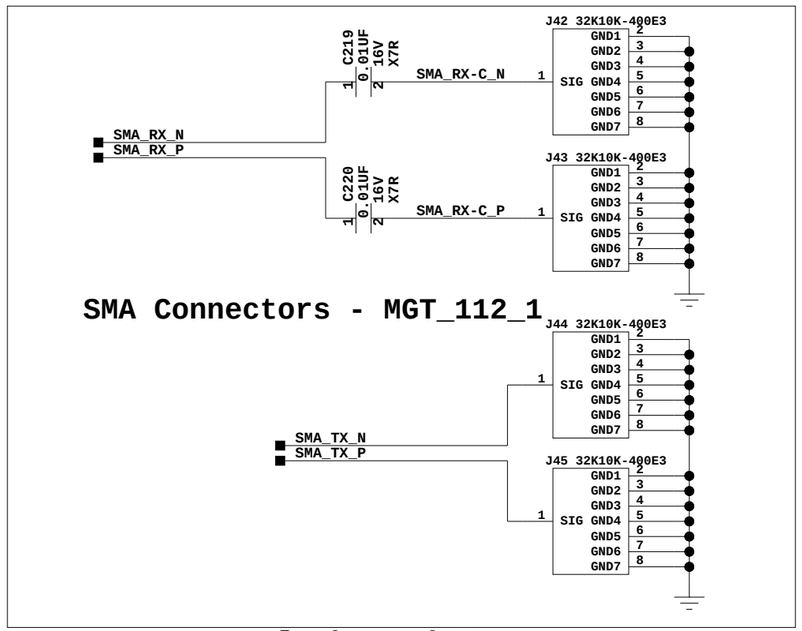
PCI-E Connectors
MGT_114_0





SFP MODULE
MGT_102B





SMA Connectors - MGT_112_1

MGT Clocks and Connectors

Title:	MGT Connectors SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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MGT PLL Regulator

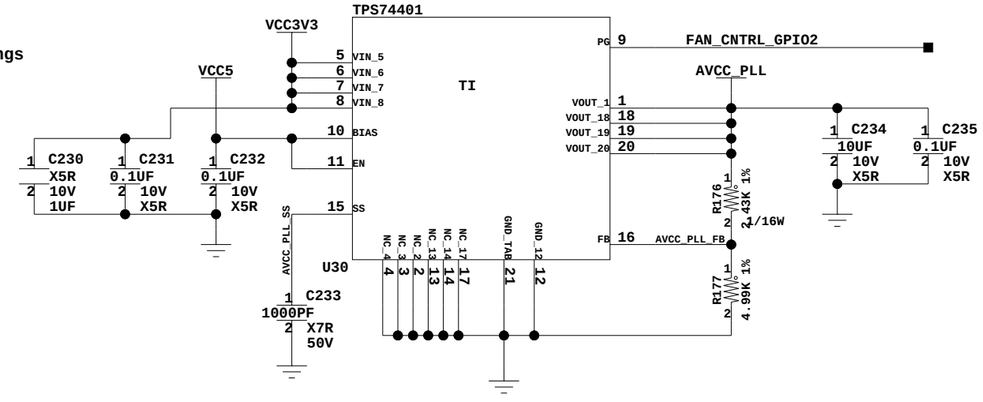
Voltage Output Settings

LXT & SXT (ML505/6)
AVCC_PLL = 1.2V @ 3A

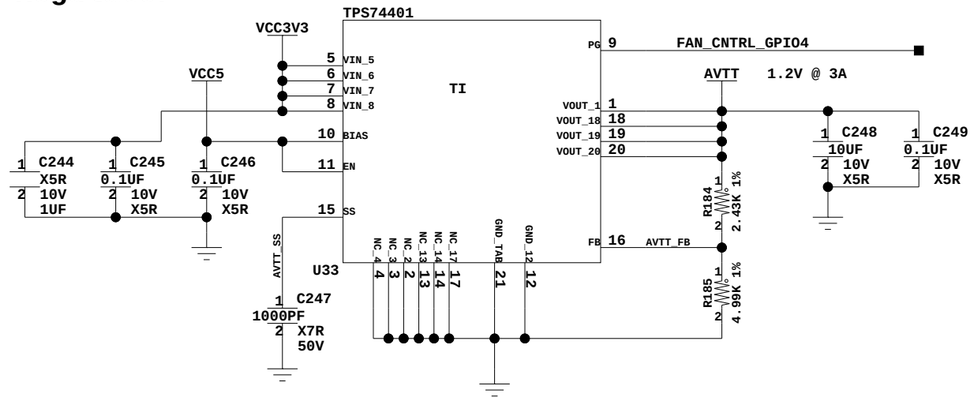
R176 = 2.43K 1%
R177 = 4.99K 1%

FXT Only (ML507)
AVCC_PLL = 1.0V @ 3A

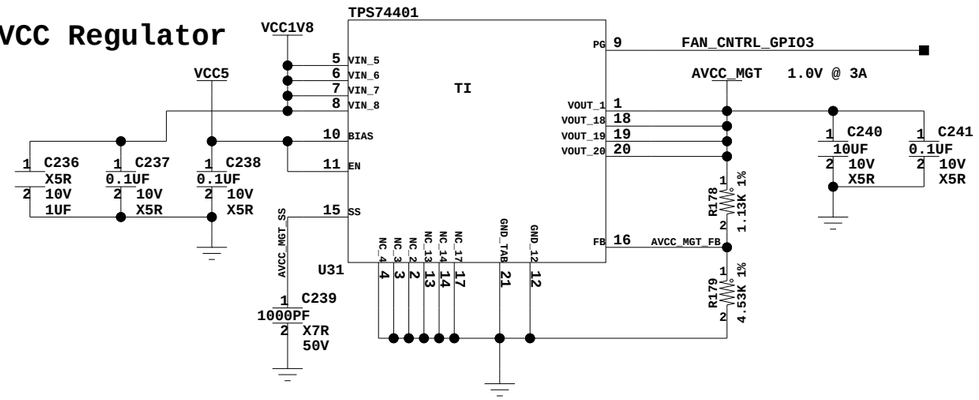
R176 = 1.13K 1%
R177 = 4.53K 1%



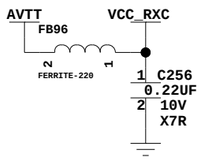
MGT VTT Regulator



MGT AVCC Regulator



MGT RXC Regulator



MGT Power Supplies

XILINX

Title:	MGT Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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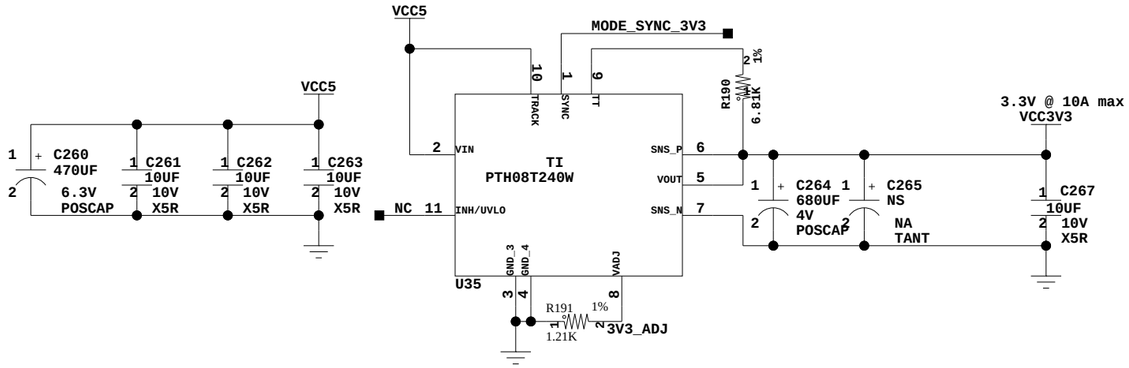
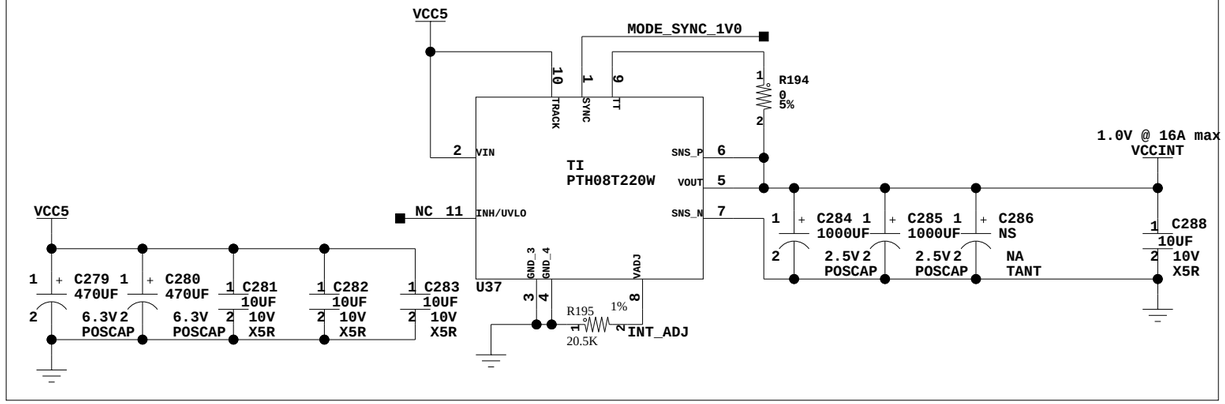
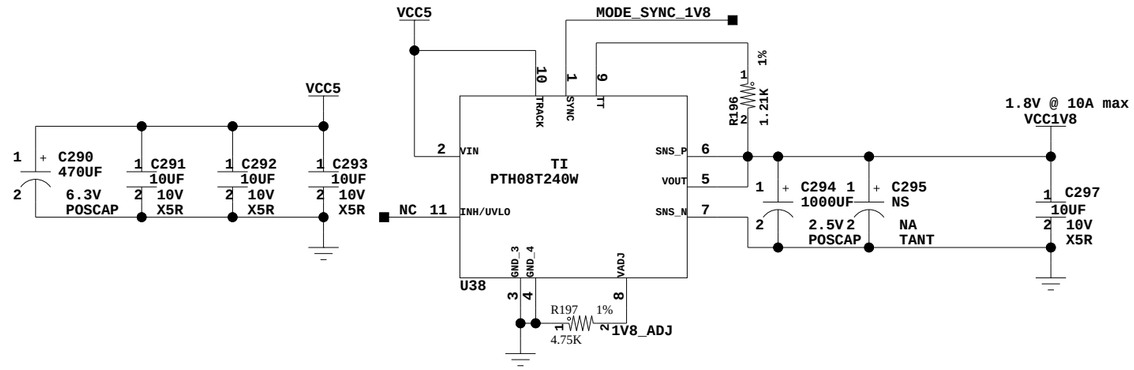
5v to 3.3V Regulator



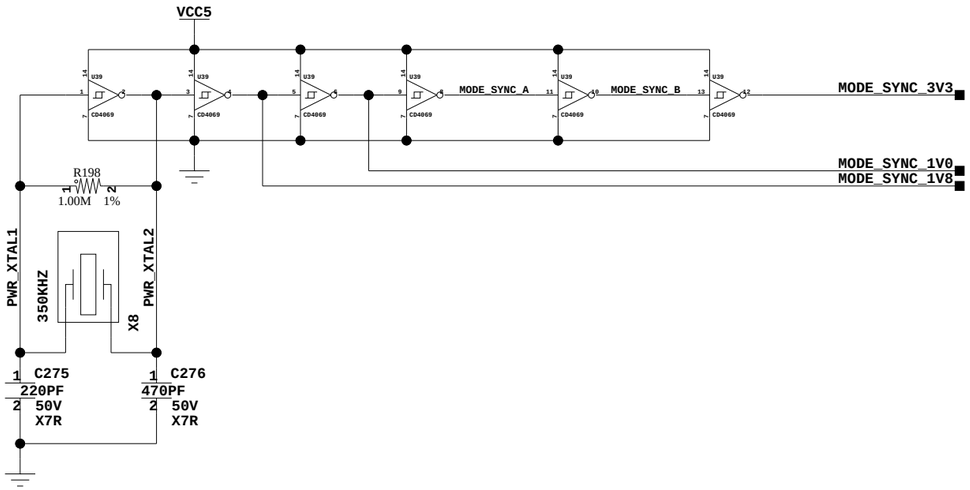
5v to 1.0V Regulator



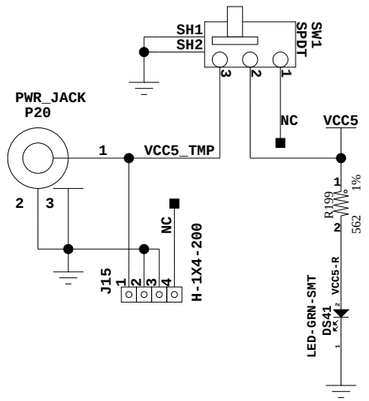
5v to 1.8V Regulator



5V Power Synchronizing Circuit



5V Power - Jack, Switch and LED



5V Power Supplies

XILINX

Title:	Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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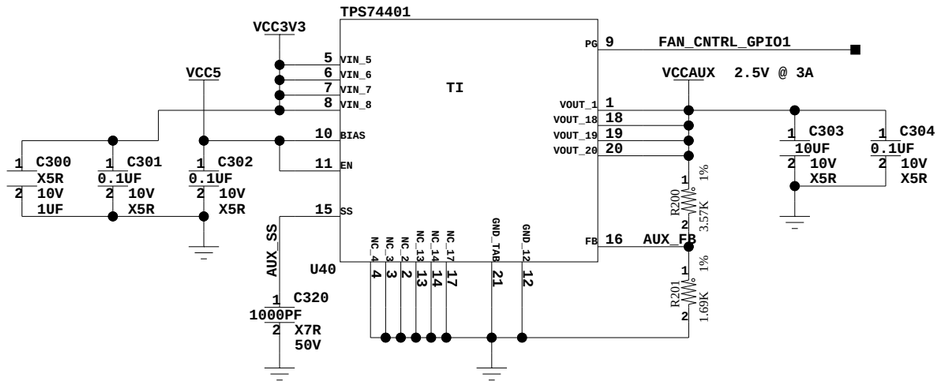
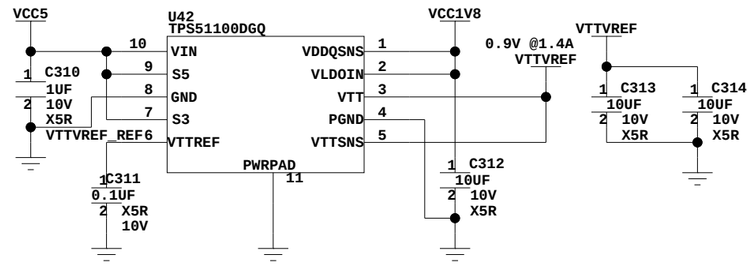
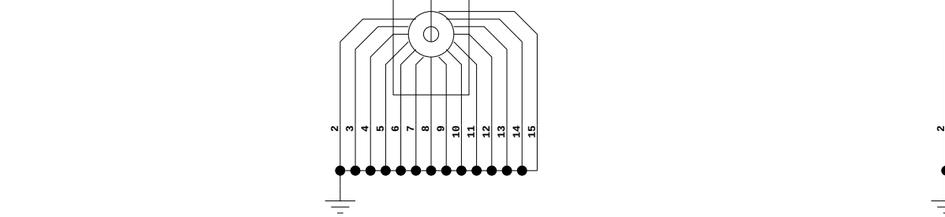
3.3v to 2.5V (VCC AUX) Regulator



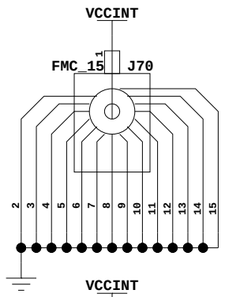
5V to 0.9V (DDR VTT VREF) Regulator

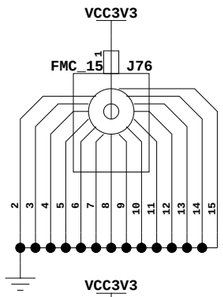


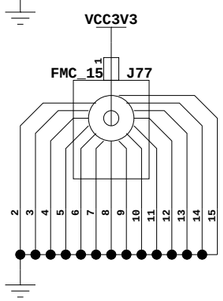
3.3v to 2.5V Regulator



5V to 0.9V (DDR2 VTT DDR) Regulator







5V and 3.3V Power Supplies

XILINX

Title:	Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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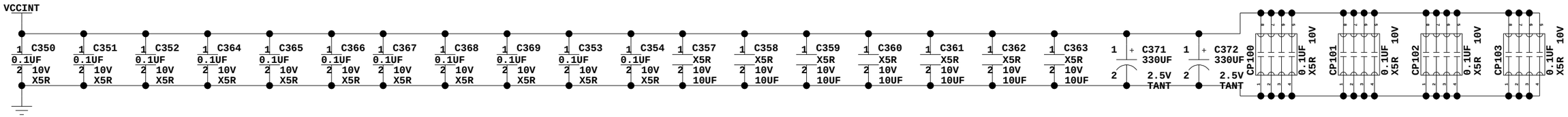
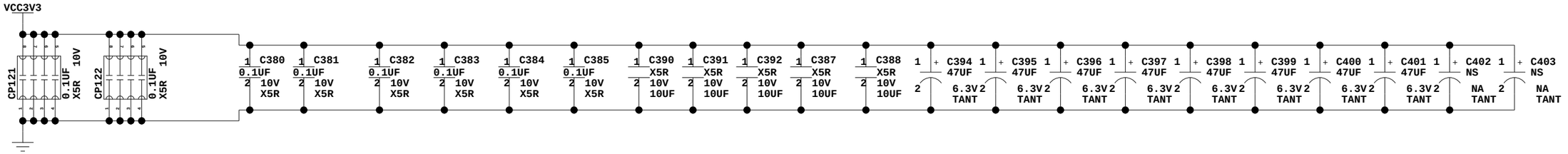
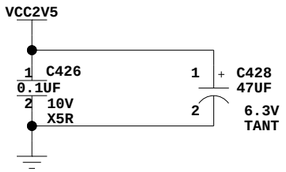
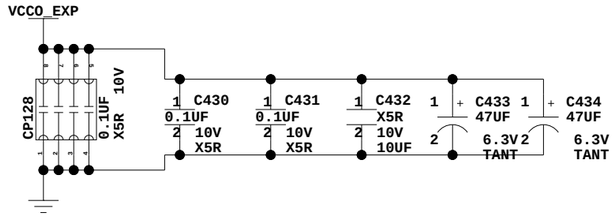
VCCINT Caps

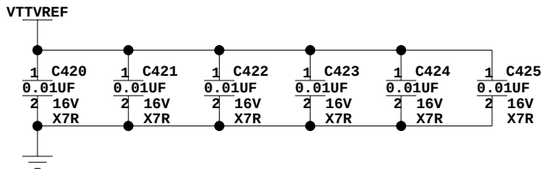


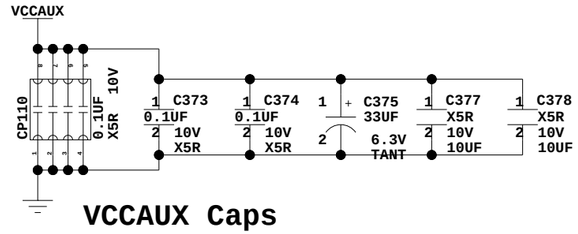
VCCO Caps



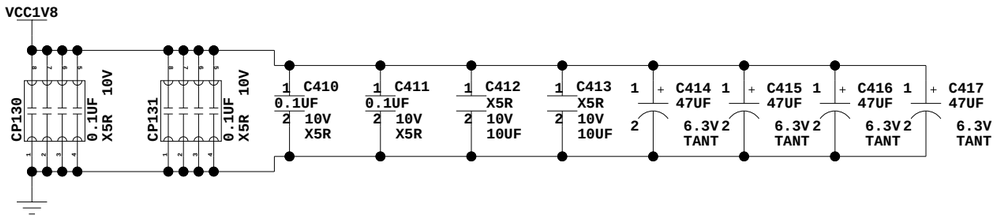








VCCAUX Caps



XILINX

Title:	FPGA Decoupling SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 27 of 27	Drawn By BP